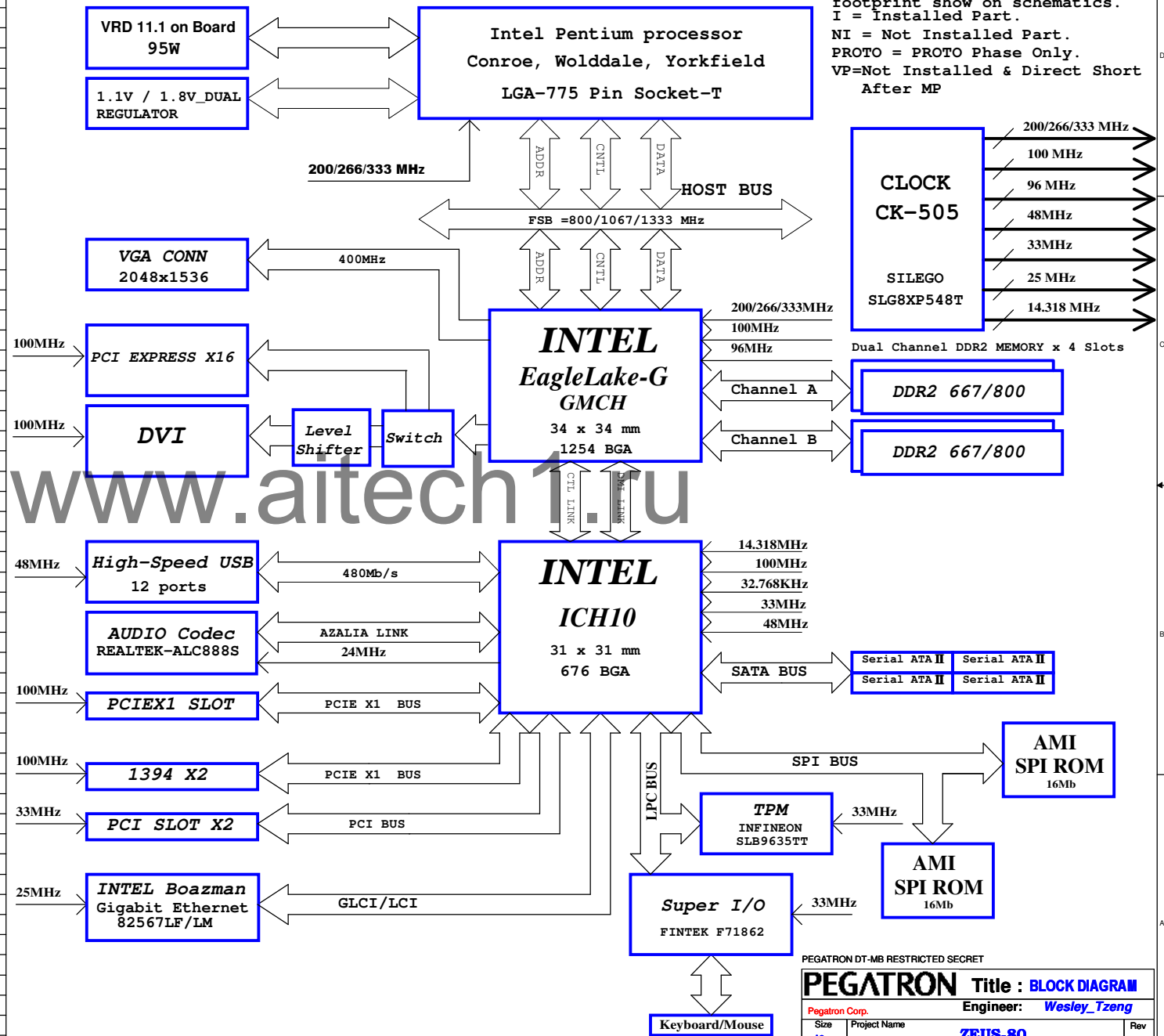


ZEUS-80

MP1.0 (R1.07)

Update 2008/8/20

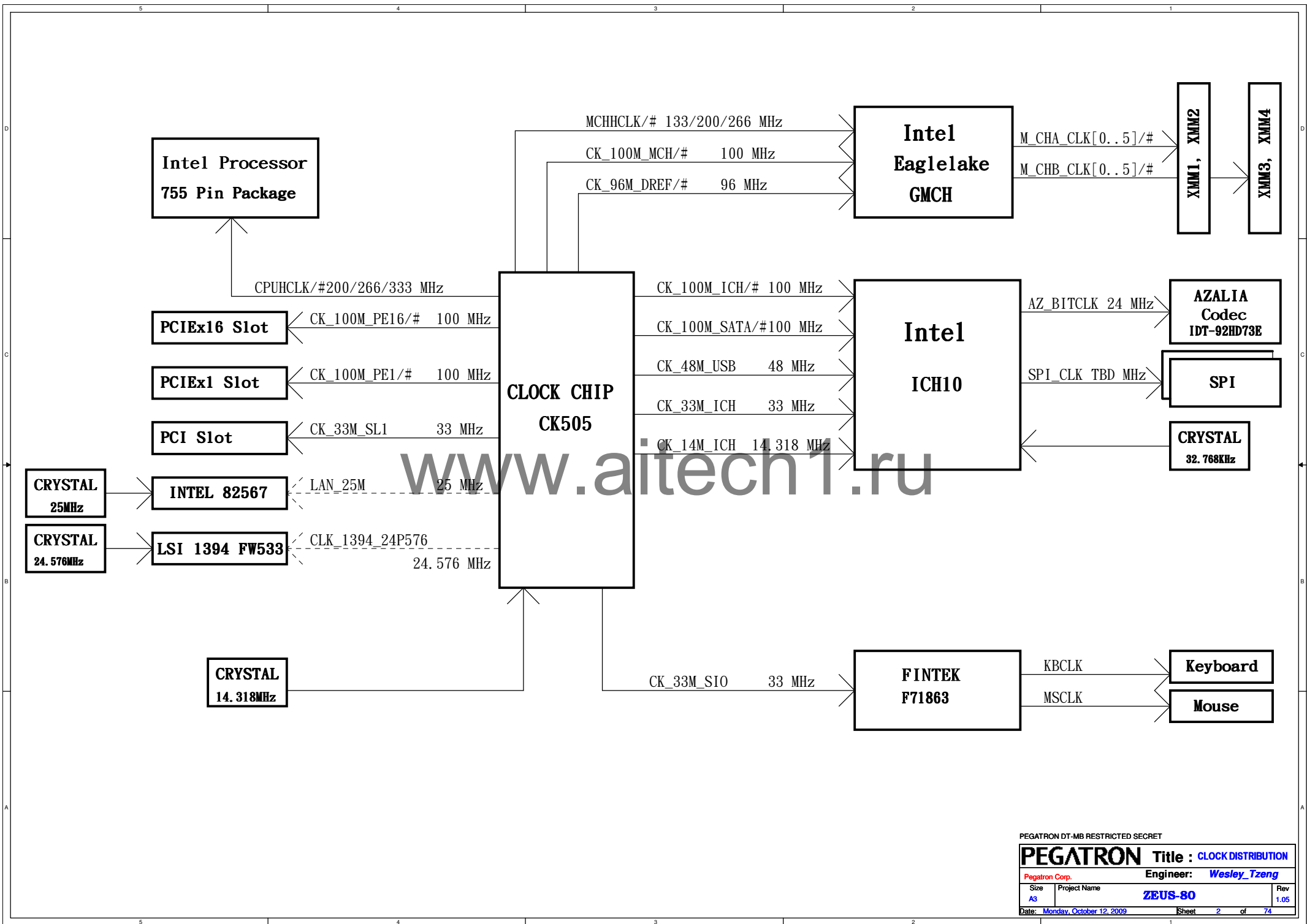
PAGE	TITLE
01	BLOCK DIAGRAM
02	CLOCK DISTRIBUTION
03	SIGNAL & RESET MAP
04	POWER FLOW
05	POWER DISTRIBUTION
06	POWER SEQUENCE
07	CLOCK SLG8XP548T
08~10	PROCESSOR LGA775 1 ~ 3
11~17	INTEL EAGLELAKE 1 ~ 7
18~19	DDR2 CHANNEL A&B
20	DDR2 TERMINATION A&B
21	INTEGRATED VGA PORT
22	DVI CONTROL
23	DVI / PCIE MUX
24	DVI LEVEL SHIFTER
25	DVI CONNECTOR
26	PCI EXPRESS X16 SLOT
27~32	INTEL ICH10
33~35	PCI EXPRESS X1 & PCI SLOT
36	REALTEK ALC888S
37	FRONT AUDIO CONNECTOR
38	REAR AUDIO CONNECTOR
39	INTEL 82567 LAN
40	RJ45+USB CONNECTOR
41	USB REAR CONNECTOR
42~43	USB FRONT CONNECTOR
44	JMB381 CONTROLLER
45	1394 CONNECTOR
46	SATA and eSATA
47	SPI SERIAL FLASH
48~49	SUPER I/O F71862 1 ~ 2
50	PARALLEL PORT
51	SERIAL PORT X2
52	PS2 KB & MS CONNECTOR CPC
53	FAN CIRCUIT FOR 4 - PIN
54	H/W MONITOR
55	PANEL
56	ITP 31P DEBUG CONNECTOR
57	ATX POWER 24P CONNECTOR
58	CLINK PWROK
59	TPM SLB9635TT
60	+5V_USB_R & +5V_USB_L
61	+1P1V CORE
62	+1P1V_FSB_VTT
63	+1P8V_DUAL
64	VCORE CONTROLLER
65	VCORE DRIVER 1
66	VCORE DRIVER 2
67	+3P3VSB & +1P1V_VR & +1P1V_CL
68	+5V_DUAL
69	+3P3V_CL&1P5V_ICH
70	ECN CONTROL TABLE
71~74	CHANGE HISTORY 1~4



CAD Note:
 Default component footprint is SMD 0402 type. Difference footprint show on schematics.
 I = Installed Part.
 NI = Not Installed Part.
 PROTO = PROTO Phase Only.
 VP=Not Installed & Direct Short After MP

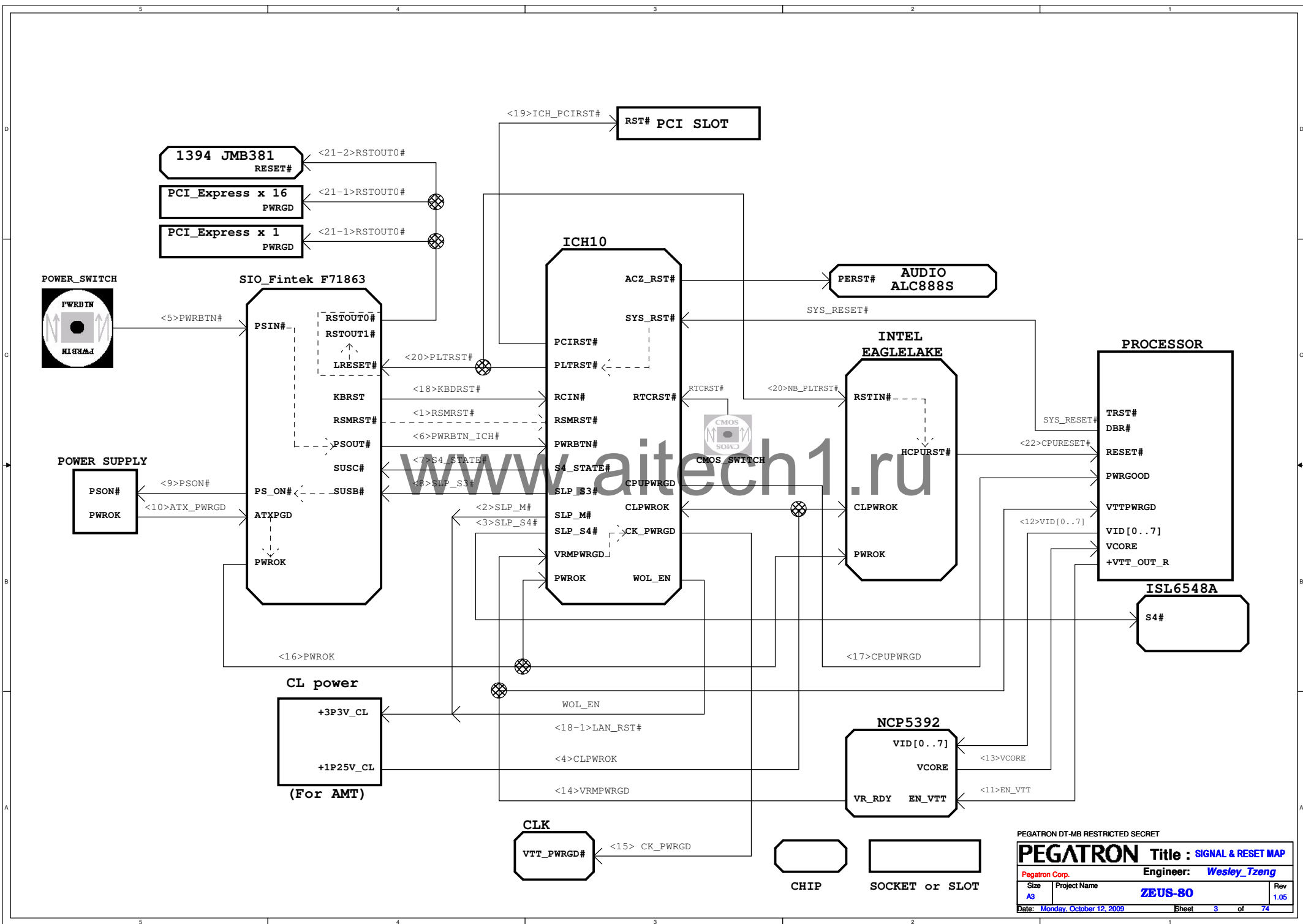
PEGATRON DT-MB RESTRICTED SECRET

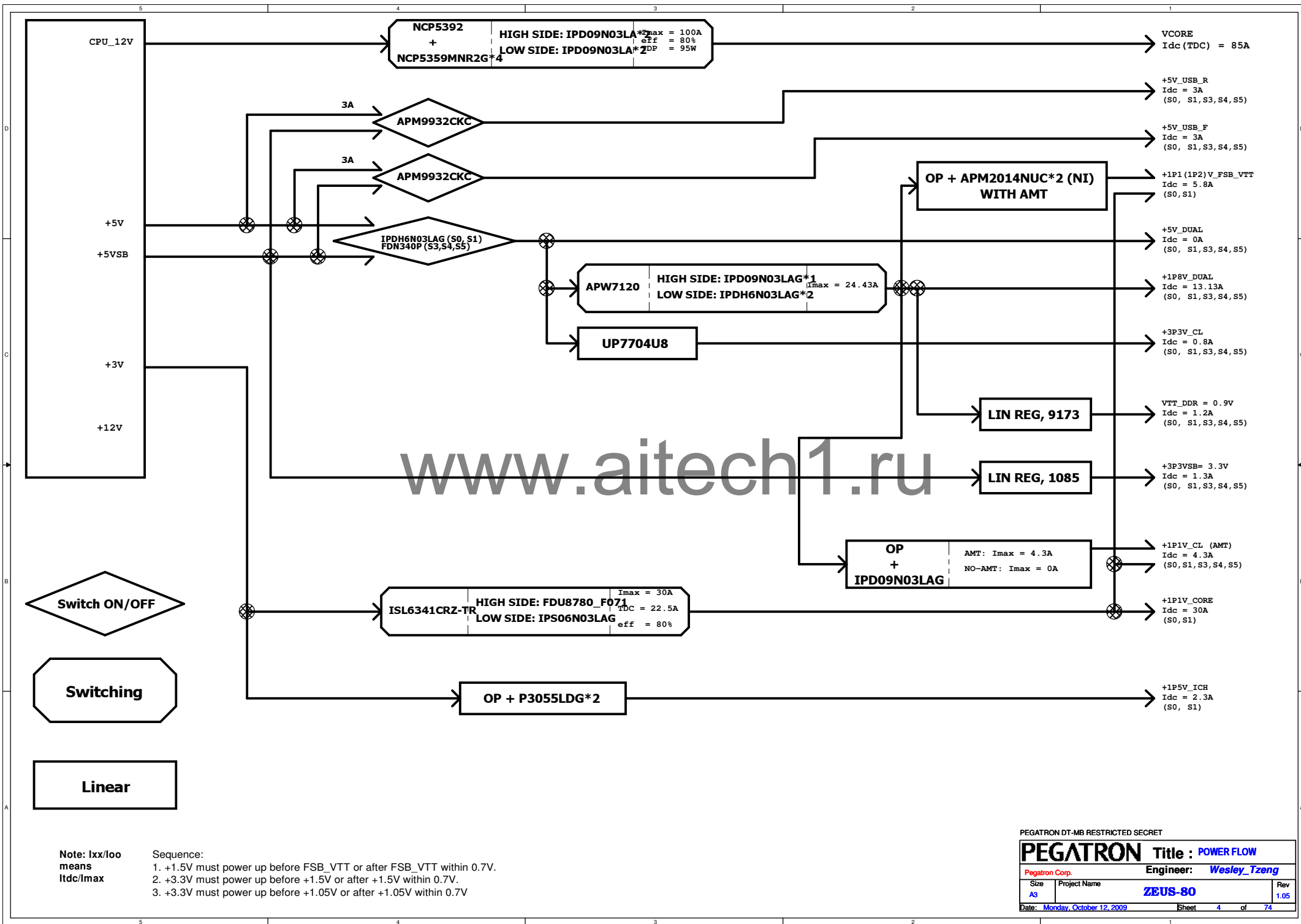
PEGATRON		Title : BLOCK DIAGRAM	
Pegatron Corp.		Engineer: Wesley_Tzeng	
Size A3	Project Name ZEUS-80	Rev 1.05	
Date: Monday, October 12, 2009		Sheet 1 of 74	



PEGATRON DT-MB RESTRICTED SECRET

PEGATRON		Title : CLOCK DISTRIBUTION	
Pegatron Corp.		Engineer: Wesley_Tzeng	
Size A3	Project Name ZEUS-80	Rev 1.05	
Date: Monday, October 12, 2009		Sheet 2	of 74

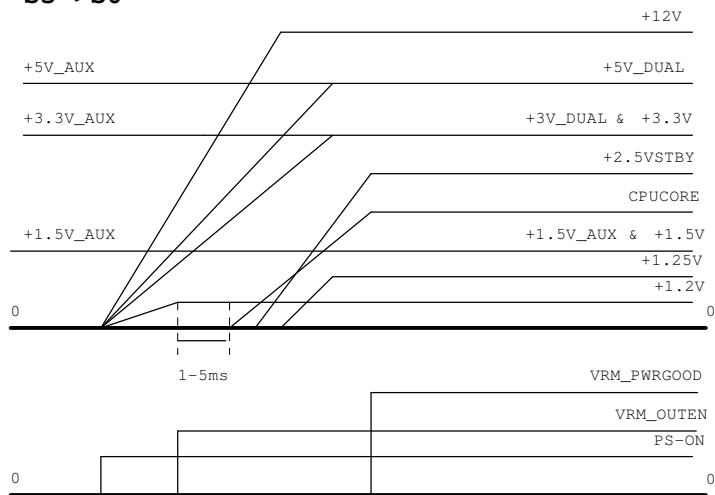




PEGATRON DT-MB RESTRICTED SECRET

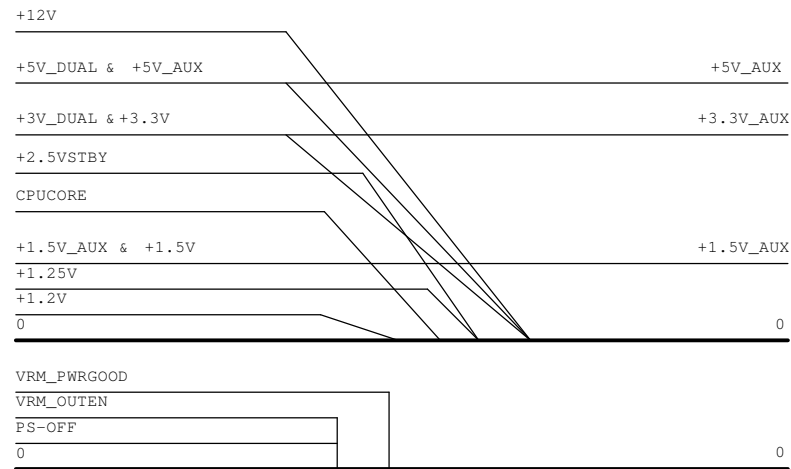
PEGATRON		Title : POWER FLOW	
Pegatron Corp.		Engineer: Wesley_Tzeng	
Size A3	Project Name ZEUS-80	Rev 1.05	
Date: Monday, October 12, 2009		Sheet 4 of 74	

S5→S0

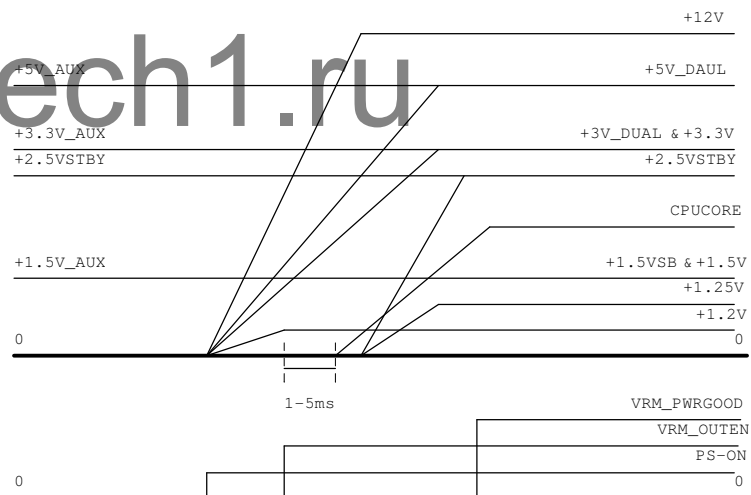


- 1.CPUCORE must rise after the voltage across 90% of +1.2V,andthe interval is within 1-5ms
- 2.VRM_OUTEN rises after the voltage across 90% of its specified value

S0→S5

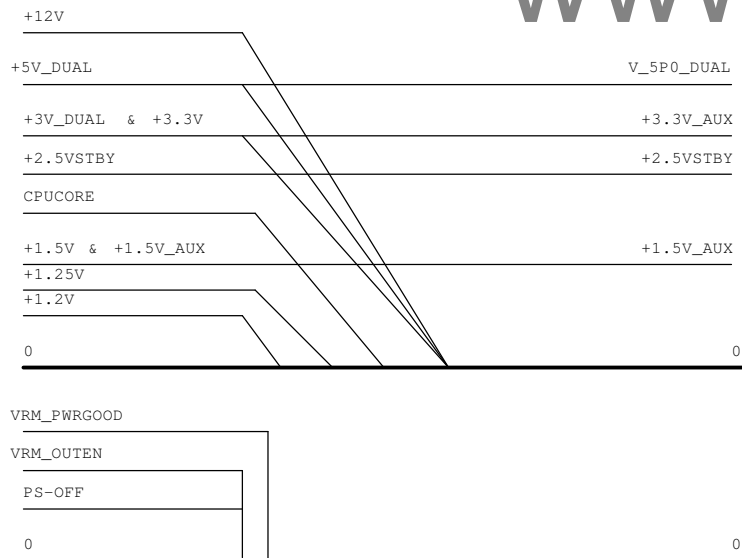


S3→S0



- 1.CPUCORE must rise after the voltage across 90% of +1.2V,andthe interval is within 1-5ms
- 2.VRM_OUTEN rises after the voltage across 90% of its specified value

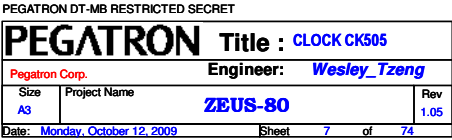
S0→S3

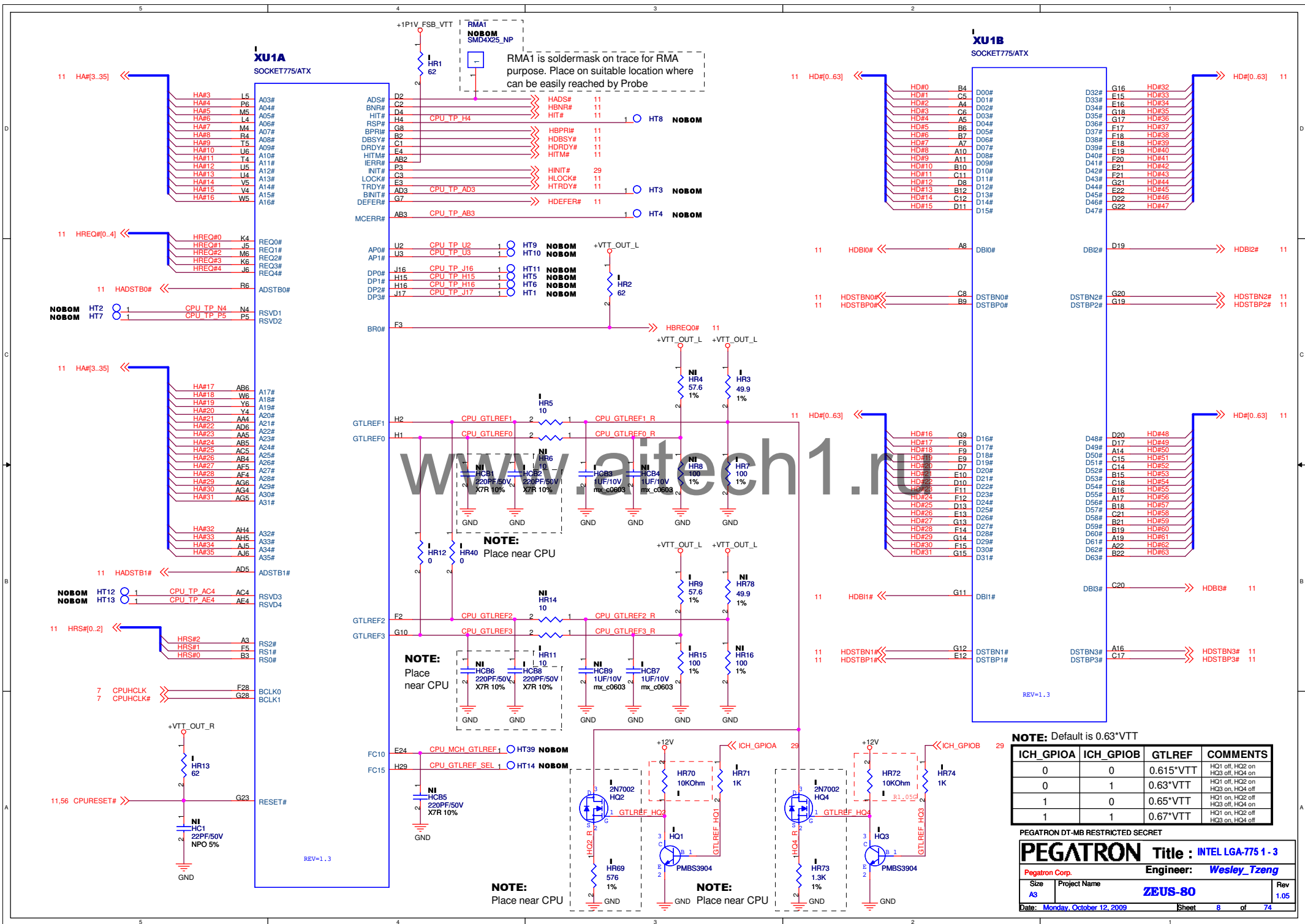


- S0:** Windows Running+12V,V_5P0_DUAL,+3.3V,+3.3V_AUX,+2.5VSTBY,CPUCORE,+1.5V,+1.5V_AUX,+1.25V,+1.2V existed
S3: Windows StandbyV_5P0_DUAL,+3.3V_AUX,+1.5V_AUX,+2.5VSTBY existed
S5: AC Power On Only+5V_AUX,+3.3V_AUX,+1.5V_AUX existed

PEGATRON DT-MB RESTRICTED SECRET

PEGATRON		Title : POWER SEQUENCE	
Pegatron Corp.		Engineer: Wesley_Tzeng	
Size A3	Project Name ZEUS-80	Rev 1.05	
Date: Monday, October 12, 2009		Sheet 6	of 74





[illegible]

The schematic diagram illustrates the electrical connections for the NOBOM board. Key components and their connections are as follows:

- Power and Ground Connections:**
 - +VTT_OUT_R:** Connected to pins 1, 3, 5, and 7 of the HRN1A, HRN1B, HRN1C, and HRN1D components.
 - +VTT_OUT_R:** Connected to pins 1, 3, 5, and 7 of the HRN2A, HRN2B, HRN2C, and HRN2D components.
 - +VTT_OUT_R:** Connected to the top terminal of the HR65 680 resistor.
 - GND:** Connected to the bottom terminal of the HR65 680 resistor.
 - +VCCORE:** Connected to the top terminal of the HCB16 component.
 - GND:** Connected to the bottom terminal of the HCB16 component.
- Signal Connections:**
 - RCVID[0..7]:** Connected to pins 2, 4, 6, and 8 of the HRN1A, HRN1B, HRN1C, and HRN1D components.
 - VID_SELECT:** Connected to pins 2, 4, 6, and 8 of the HRN2A, HRN2B, HRN2C, and HRN2D components.
 - SKTOCC#:** Connected to pin 1 of the HCB16 component.
 - TRD_CPU_P and TRD_CPU_N:** Connected to pins 2 and 1 of the HCB16 component.
 - VCC_MB_SENSE:** Connected to pin 1 of the HCB16 component.
 - VSS_MB_SENSE:** Connected to pin 2 of the HCB16 component.
 - VCC_SEN AN3:** Connected to pin 1 of the HCB16 component.
 - VSS_SEN AN4:** Connected to pin 2 of the HCB16 component.
 - VCC_D_SEN:** Connected to pin 1 of the HCB16 component.
 - VSS_D_SEN:** Connected to pin 2 of the HCB16 component.
- Component Values:**
 - HR65 680:** Resistor value.
 - HCB16:** Component value.
 - 100PF/50V:** Capacitor value.

2 SMI#
 2 A20M#
 2 FERR#/PBE#
 2 LINT0
 2 LINT1
 2 IGNNE#
 2 STPCLK#
 3
 3 VCCA
 3
 3
 3 VSSA
 3
 3
 3 VCCIOPLL

[illegible]

LL_ID1 AA2 CPU_LL ID1

LL_ID0 V2 CPU_LL ID0 1 HT29 NOBOM

BOOTSELECT Y1 CPU_BOOT

NC AL3 VRDSEL 1 HT30 NOBOM

1 HR5 51

Diagram showing the connection for Pin 29 (PECE). The signal is connected to G5 (PECE) and F6 (IMPSEL F6). The pin is also connected to GND.

HR56 51 +VTT_OUT_R +VTT_OUT_L +VTT_OUT_R

FORCEPR#	AK6	HFORCEPH#	1%	1%
N1	CPUPOWERD			

PWRGOOD M1 **PROCHOT#**
 PROCHOT# AL2 **PROCHOT#**
 HERMTRIP# M2 **HERMTRIP#**

THERMALTRIP# NEED A PULL UP RESISTOR N

The schematic diagram illustrates the ADI reference design for the ADXL345. It shows the ADXL345 chip connected to an ADI reference design. The ADXL345 is a 3-axis digital accelerometer. The ADI reference design is a custom PCB. The schematic shows the following connections: VDD to VDD, GND to GND, SDA to SDA, SCL to SCL, and the 3-axis outputs to the ADI reference design. The ADI reference design is a custom PCB. The schematic shows the following connections: VDD to VDD, GND to GND, SDA to SDA, SCL to SCL, and the 3-axis outputs to the ADI reference design.

[illegible]

HR60 1 51 2

NOBOM HT18

NOBOM HT19

NOBOM HT20

NOBOM HT27

NOBOM HT28

CPU TP N5 N5

CPU TP E7 E7

CPU TP A5 A5

CPU TP D16 D16

CPU TP A20 A20

CPU TP E23 E23

RSVD17

RSVD18

RSVD19

RSVD20

RSVD22

RSVD23

RSVD31

+VTT_OUT_R

HR52

BOOTSELECT:
Install PD resistor to
prevent PSC SMC CDM PST.

Prevents USB and SATA ports from booting

NPO 5%

GND

HR57 1 2 470

7,14 FSBSEL0
7,14 FSBSEL1
7,14 FSBSEL2

G29 H30 BSEL0
G30 BSEL1
BSEL2

— HFORCEPH# 64

```

    << CPUPWRGD 30
    >> PROCHOT# 30,64
    >> H_THMTRIP# 29

```

PEGATR

PE

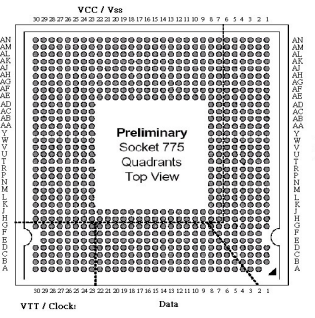
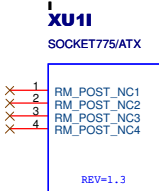
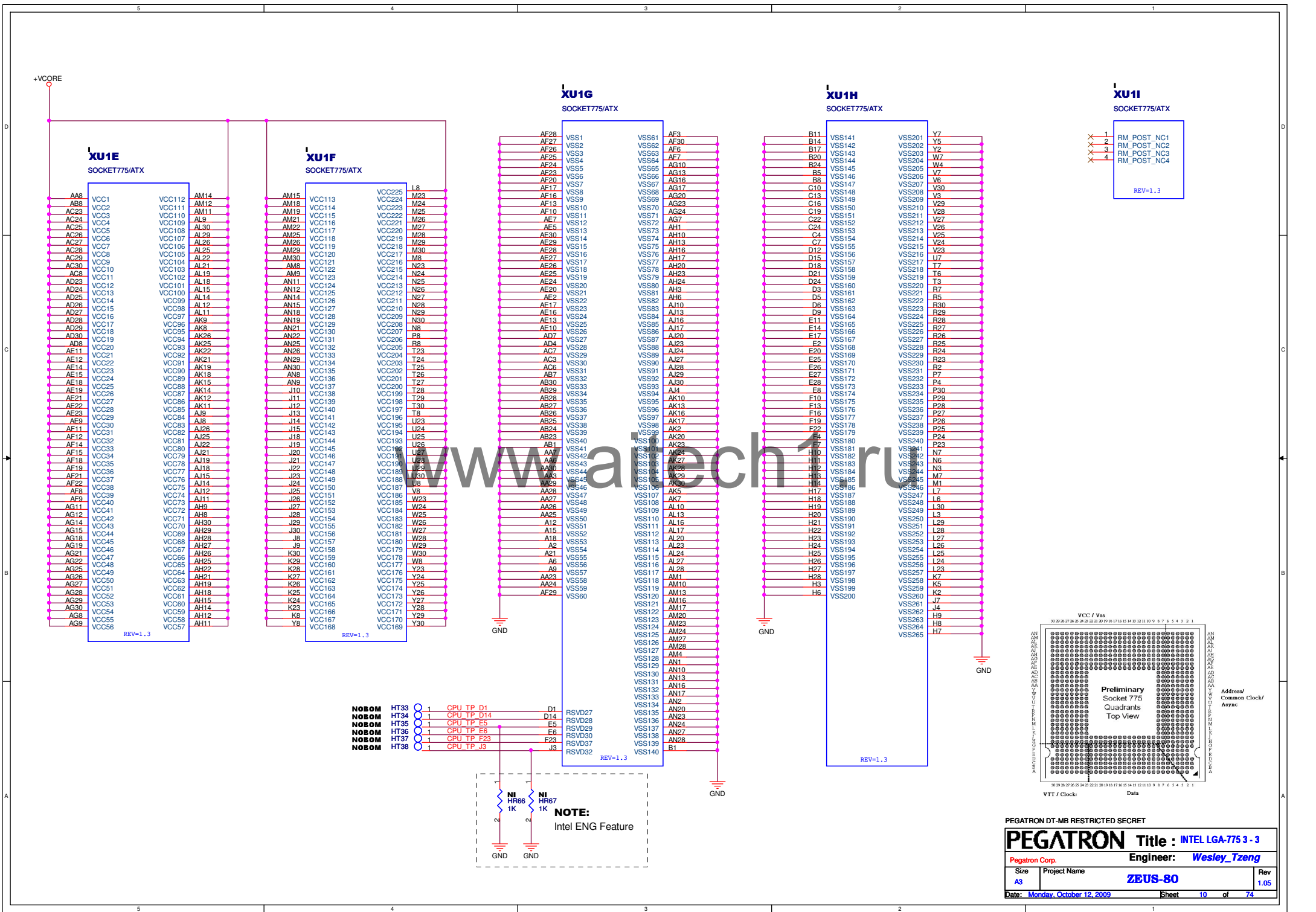
HCB14 0.01UF/25V X7R 10% HCB15 10UF/6.3V X5R 10% mx_c0805

GND GND

27 >> VTT_SELECT 62

100

PEGATRON DT-MB RESTRICTED SECRET			
PEGATRON		Title : INTEL LGA-775 2 - 3	
Pegatron Corp.		Engineer: Wesley_Tzeng	
Size A3	Project Name ZEUS-80		Rev 1.05
Date: Monday, October 12, 2009		Sheet	9 of 74



18,20 M_CHA_MAA[0..14] <<

18,20 M_CHA_WE# <<
18,20 M_CHA_CAS# <<
18,20 M_CHA_RAS# <<

18,20 M_CHA_BA0 <<
18,20 M_CHA_BA1 <<
18,20 M_CHA_BA2 <<

18,20 M_CHA_CS#0 <<
18,20 M_CHA_CS#1 <<
18,20 M_CHA_CS#2 <<
18,20 M_CHA_CS#3 <<

18,20 M_CHA_CKE0 <<
18,20 M_CHA_CKE1 <<
18,20 M_CHA_CKE2 <<
18,20 M_CHA_CKE3 <<

18,20 M_CHA_ODT0 <<
18,20 M_CHA_ODT1 <<
18,20 M_CHA_ODT2 <<
18,20 M_CHA_ODT3 <<

18 M_CHA_CLK0 <<
18 M_CHA_CLK0# <<
18 M_CHA_CLK1 <<
18 M_CHA_CLK1# <<
18 M_CHA_CLK2 <<
18 M_CHA_CLK2# <<
18 M_CHA_CLK3 <<
18 M_CHA_CLK3# <<
18 M_CHA_CLK4 <<
18 M_CHA_CLK4# <<
18 M_CHA_CLK5 <<
18 M_CHA_CLK5# <<

M_CHA_MAA0 BC41
M_CHA_MAA1 BC35
M_CHA_MAA2 BB32
M_CHA_MAA3 BC32
M_CHA_MAA4 BD32
M_CHA_MAA5 BB31
M_CHA_MAA6 BA31
M_CHA_MAA7 BD31
M_CHA_MAA8 BD30
M_CHA_MAA9 AW43
M_CHA_MAA10 BC30
M_CHA_MAA11 BB30
M_CHA_MAA12 AM42
M_CHA_MAA13 AM42
M_CHA_MAA14 BD28

NU1C

AW42 SWE_A#
AU42 SCAS_A#
AV42 SRAS_A#
AV45 SBS_A0
AY44 SBS_A1
BC28 SBS_A2
AU43 SCS_A0#
AR40 SCS_A1#
AU44 SCS_A2#
AM43 SCS_A3#
BB27 SCKE_A0
BD27 SCKE_A1
BA27 SCKE_A2
AY26 SCKE_A3
AR42 SODT_A0
AM44 SODT_A1
AR44 SODT_A2
AL40 SODT_A3

AY37 SCLK_A0
BA37 SCLK_A0#
AW29 SCLK_A1
AY29 SCLK_A1#
AU37 SCLK_A2
AU37 SCLK_A2#
AU33 SCLK_A3
AT33 SCLK_A3#
AT30 SCLK_A4
AR30 SCLK_A4#
AW38 SCLK_A5
AY38 SCLK_A5#

DDR_A

SDQS_A0 BC5
SDQS_A0# BD4
SDM_A0 BC3
SDQ_A0 BC2
SDQ_A1 BD3
SDQ_A2 BD7
SDQ_A3 BB7
SDQ_A4 BB2
SDQ_A5 BA3
SDQ_A6 BE6
SDQ_A7 BD6
SDQS_A1 BB9
SDQS_A1# BC9
SDM_A1 BD9
SDQ_A8 BB8
SDQ_A9 AY8
SDQ_A10 BD11
SDQ_A11 BB11
SDQ_A12 BC7
SDQ_A13 BE8
SDQ_A14 BD10
SDQ_A15 AY11
SDQS_A2 BD15
SDQS_A2# BR15
SDM_A2 BD14
SDQ_A16 BB14
SDQ_A17 BC14
SDQ_A18 BC16
SDQ_A19 BB16
SDQ_A20 BC11
SDQ_A21 BE12
SDQ_A22 BA15
SDQ_A23 BD16
SDQS_A3 AR22
SDQS_A3# AT22
SDM_A3 AV22
SDQ_A24 AW21
SDQ_A25 AY22
SDQ_A26 AV22
SDQ_A27 AY24
SDQ_A28 AU21
SDQ_A29 AT21
SDQ_A30 AU24
SDQ_A31 AU24
SDQS_A4 AH43
SDQS_A4# AH42
SDM_A4 AK42
SDQ_A32 AL41
SDQ_A33 AK43
SDQ_A34 AG42
SDQ_A35 AG44
SDQ_A36 AL42
SDQ_A37 AK44
SDQ_A38 AH44
SDQ_A39 AG41
SDQS_A5 AD43
SDQS_A5# AE42
SDM_A5 AE45
SDQ_A40 AF43
SDQ_A41 AF42
SDQ_A42 AC44
SDQ_A43 AC42
SDQ_A44 AF40
SDQ_A45 AF44
SDQ_A46 AD44
SDQ_A47 AC41
SDQS_A6 Y43
SDQS_A6# Y42
SDM_A6 AA45
SDQ_A48 AB43
SDQ_A49 AA42
SDQ_A50 W42
SDQ_A51 W41
SDQ_A52 AB42
SDQ_A53 AB44
SDQ_A54 Y44
SDQ_A55 Y40
SDQS_A7 T44
SDQS_A7# T43
SDM_A7 T42
SDQ_A56 V42
SDQ_A57 U45
SDQ_A58 R40
SDQ_A59 P44
SDQ_A60 V44
SDQ_A61 V43
SDQ_A62 R41
SDQ_A63 R44

M_CHA_DQS0 18
M_CHA_DQS0# 18
M_CHA_DM0 18

M_CHA_DQ0 18
M_CHA_DQ1 18
M_CHA_DQ2 18
M_CHA_DQ3 18
M_CHA_DQ4 18
M_CHA_DQ5 18
M_CHA_DQ6 18
M_CHA_DQ7 18

M_CHA_DQS1 18
M_CHA_DQS1# 18
M_CHA_DM1 18

M_CHA_DQ8 18
M_CHA_DQ9 18
M_CHA_DQ10 18
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M_CHA_DQ12 18
M_CHA_DQ13 18
M_CHA_DQ14 18
M_CHA_DQ15 18

M_CHA_DQS2 18
M_CHA_DQS2# 18
M_CHA_DM2 18

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M_CHA_DQ23 18

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M_CHA_DQS3# 18
M_CHA_DM3 18

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M_CHA_DQS5# 18
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M_CHA_DQ47 18

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M_CHA_DQS6# 18
M_CHA_DM6 18

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M_CHA_DQ52 18
M_CHA_DQ53 18
M_CHA_DQ54 18
M_CHA_DQ55 18

M_CHA_DQS7 18
M_CHA_DQS7# 18
M_CHA_DM7 18

M_CHA_DQ56 18
M_CHA_DQ57 18
M_CHA_DQ58 18
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M_CHA_DQ63 18

M_CHA_DQ[0..63] 18

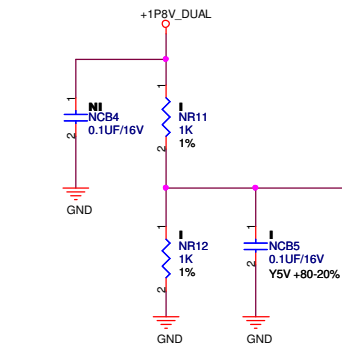
www.itech1.ru

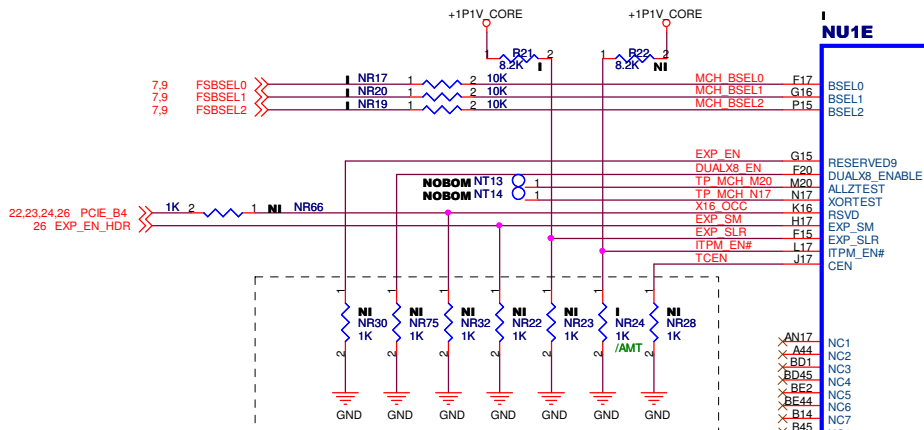
REV=1.3

EAGLELAKE

PEGATRON DT-MB RESTRICTED SECRET

PEGATRON		Title : EAGLELAKE 2-7	
Pegatron Corp.		Engineer: Wesley_Tzeng	
Size A3	Project Name ZEUS-80	Rev 1.05	
Date: Monday, October 12, 2009		Sheet 12 of 74	

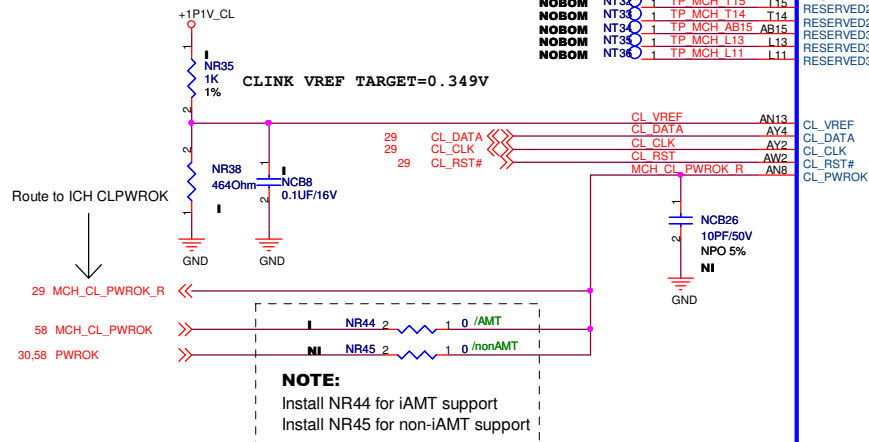




NOTE:

PIN	HIGH	LOW	DESCRIPTION
EXP_SM	CONCURRENT	NOT CONCURRENT	PCI-E/SDVO
DUALX8	1x16 PCIe	2x8 PCIe	DUALX8 ENABLE
X16_OCC	NOT PRESENCE	PRESENCE	PCIe CARD IN PRIMARY SLOT
EXP_SLR	NORMAL ATX	RESERVE BTX	PCI-E LANE RESERVAI
ITPM_EN#	DISABLE	ENABLE	iTPM Enable
TCEN	ENABLE	DISABLE	TLS CONFIDENTIALITY

NOBOM NT15	1	TP MCH M17	M17	RESERVED10
NOBOM NT16	1	TP MCH G20	G20	BSOANTEST
NOBOM NT17	1	TP MCH J16	J16	RESERVED12
NOBOM NT23	1	TP MCH M16	M16	RESERVED13
NOBOM NT18	1	TP MCH J15	J15	RESERVED14
NOBOM NT19	1	TP MCH J20	J20	RESERVED16
NOBOM NT20	1	TP MCH AR7	AR7	JTAG_TDO
NOBOM NT21	1	TP MCH AN10	AN10	JTAG_TDI
NOBOM NT22	1	TP MCH AN11	AN11	JTAG_TMS
NOBOM NT23	1	TP MCH B31	B31	RESERVED22
NOBOM NT24	1	TP MCH B32	B32	RESERVED23
NOBOM NT25	1	TP MCH U30	U30	RESERVED24
NOBOM NT26	1	TP MCH U31	U31	RESERVED25
NOBOM NT30	1	TP MCH R15	R15	RESERVED26
NOBOM NT31	1	TP MCH R14	R14	RESERVED27
NOBOM NT32	1	TP MCH T15	T15	RESERVED28
NOBOM NT33	1	TP MCH T14	T14	RESERVED29
NOBOM NT34	1	TP MCH AB15	AB15	RESERVED30
NOBOM NT35	1	TP MCH L13	L13	RESERVED32
NOBOM NT36	1	TP MCH L11	L11	RESERVED33



MISC

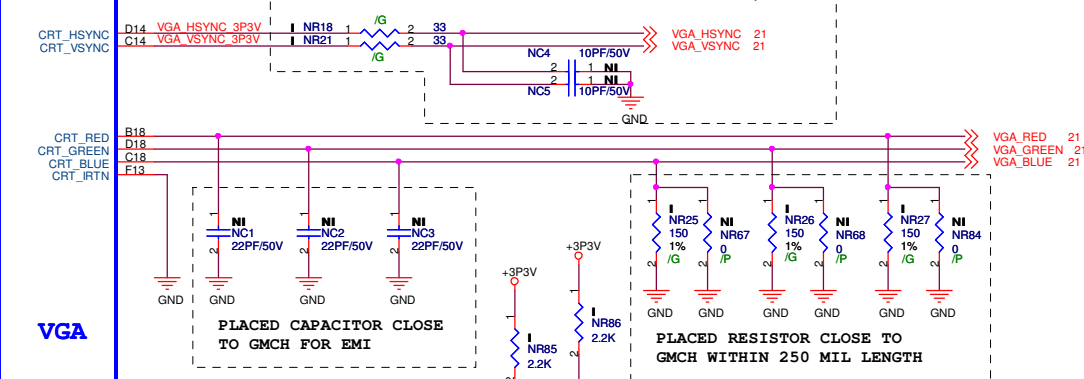
DDPC_CTRLCLK
DDPC_CTRLDATA

TEST0
TEST1
TEST2
TEST3

REV=1.3

NOTE:

Install NR67 NR68 NR84 and NOT Install NR18 NR21 for non-Graphics SKU



NOTE:

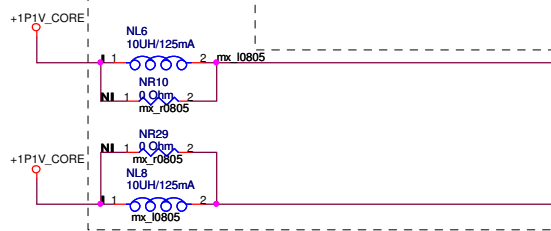
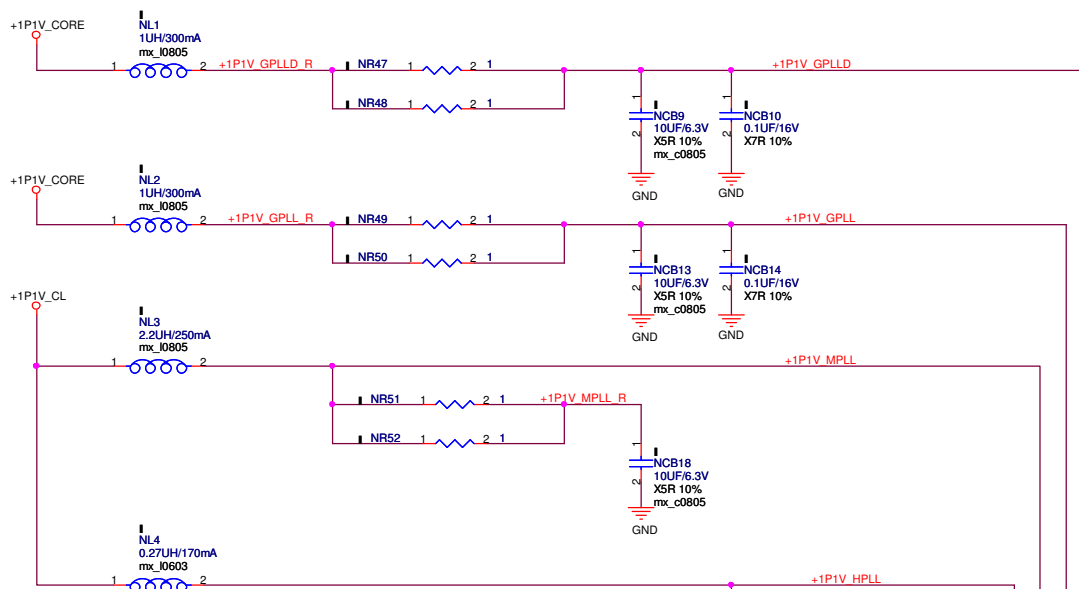
HDMI PORTC DDC Control CLK
HDMI PORTC DDC Control DATA

NOTE:

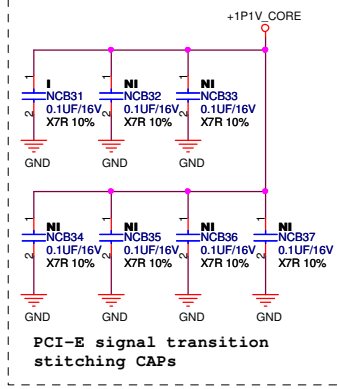
NR69 NR46 place near CPU side

PEGATRON DT-MB RESTRICTED SECRET

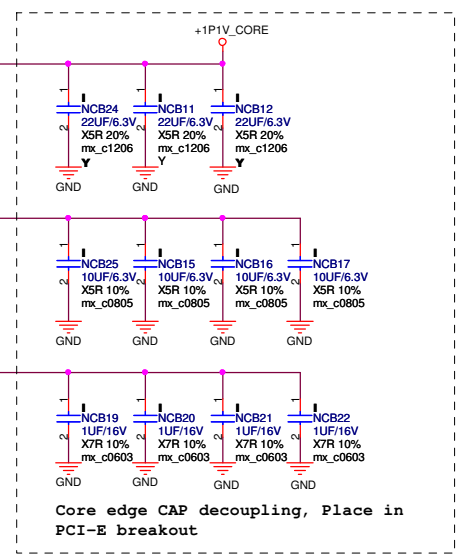
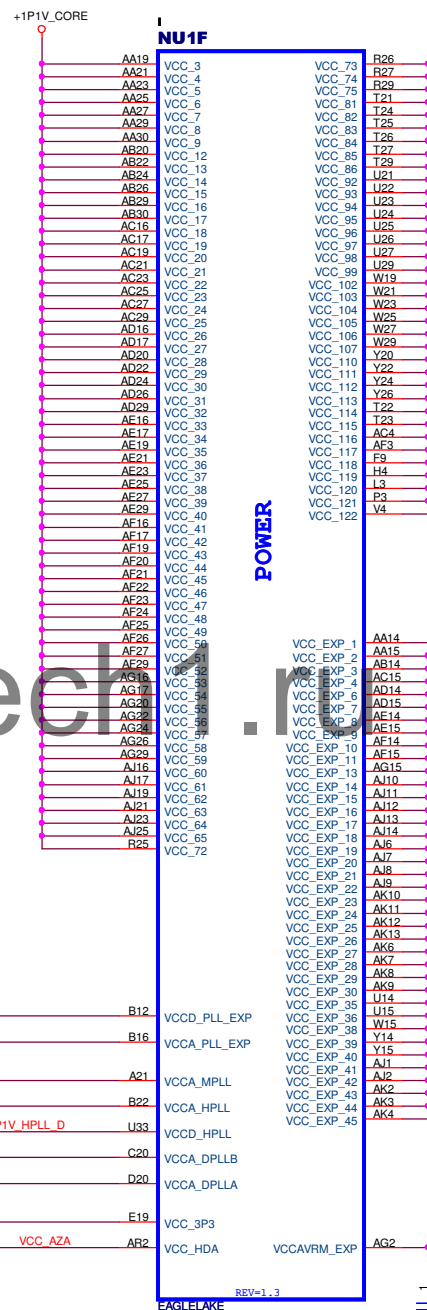
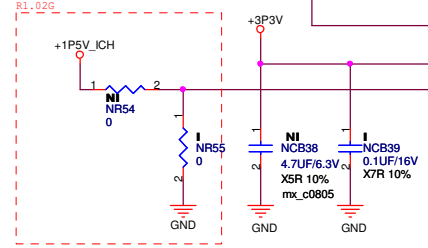
PEGATRON		Title : EAGLELAKE-7	
Pegatron Corp.		Engineer: Wesley_Tzeng	
Size A3	Project Name ZEUS-80	Rev 1.05	
Date: Monday, October 12, 2009		Sheet 14 of 74	



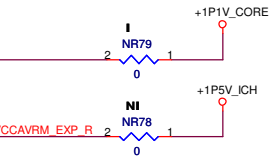
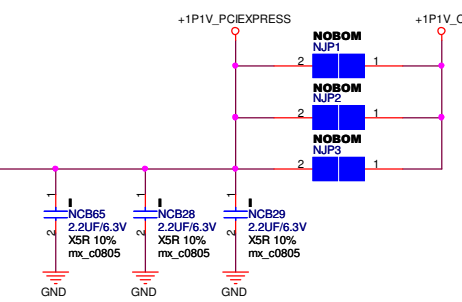
NOTE:
Change NL6,NL8 to NR10,NR29 for NON GRAPGIC SKU
NI NCE1 NCE2 NCB27 NCB30 for NON GRAPGIC SKU

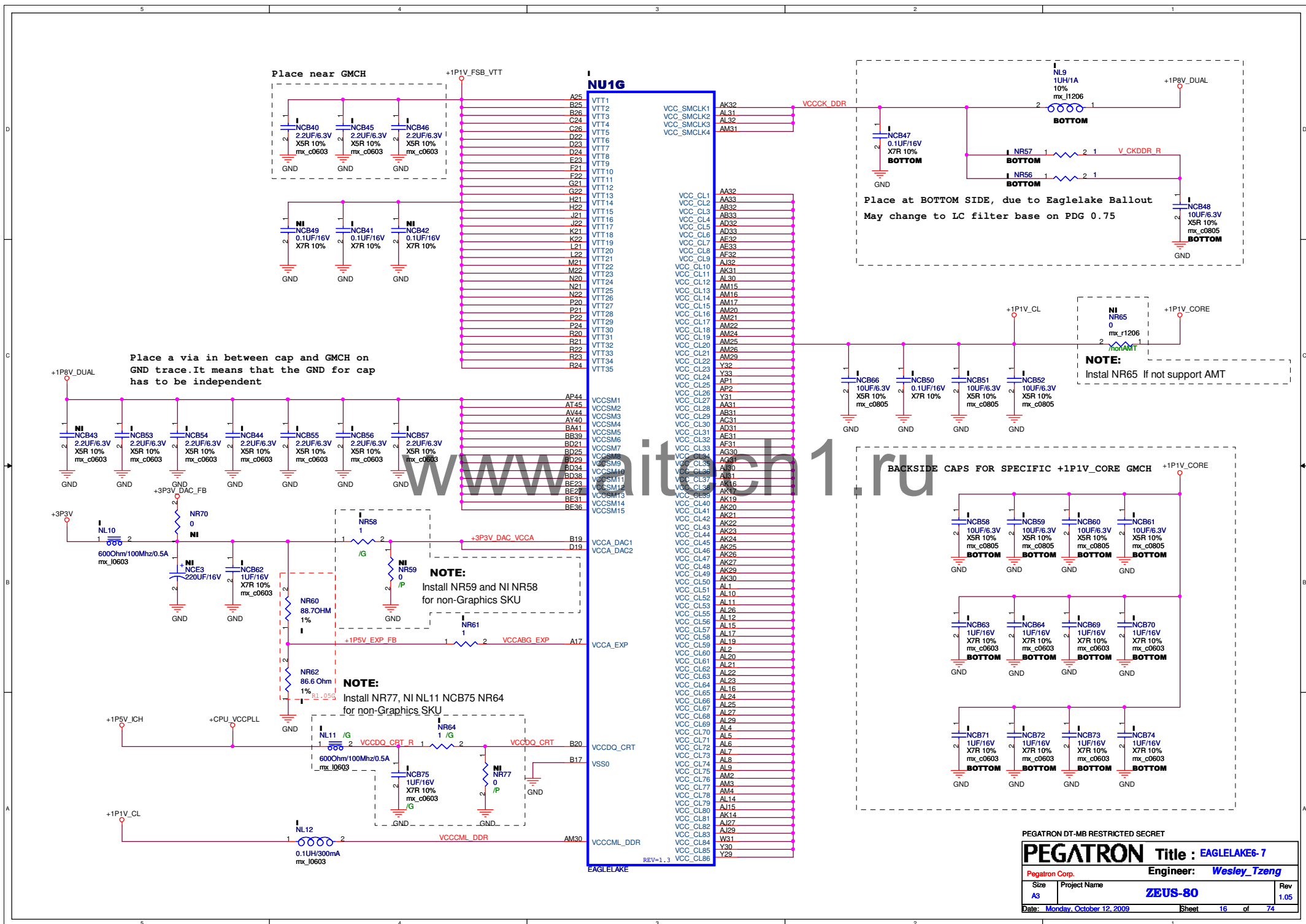


PCI-E signal transition stitching CAPs



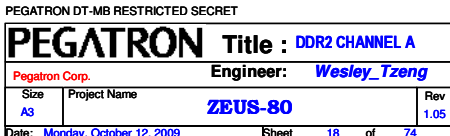
Core edge CAP decoupling, Place in PCI-E breakout





NU1H

A12	VSS1	AP20
A15	VSS2	AP22
A27	VSS3	AP24
A31	VSS4	AP29
A36	VSS5	AP45
A40	VSS6	AR10
AA1	VSS7	AR11
AA12	VSS8	AR13
AA13	VSS9	AR16
AA20	VSS10	AR26
AA22	VSS11	AR3
AA24	VSS12	AR31
AA26	VSS13	AR33
AA34	VSS14	AR35
AA38	VSS15	AR39
AA44	VSS16	AR8
AA48	VSS17	AR9
AB11	VSS18	AT1
AB12	VSS19	AT11
AB19	VSS20	AT17
AB21	VSS21	AT2
AB23	VSS22	AT24
AB25	VSS23	AT29
AB27	VSS24	AT3
AB34	VSS25	AT35
AB36	VSS26	AT39
AB39	VSS27	AT4
AB4	VSS28	AT45
AB6	VSS29	AT5
AB7	VSS30	AT52
AB9	VSS31	AT55
AC20	VSS32	AT59
AC22	VSS33	AT6
AC24	VSS34	AT62
AC3	VSS35	AT66
AD12	VSS36	AT69
AD19	VSS37	AT7
AD21	VSS38	AT72
AD23	VSS39	AT75
AD25	VSS40	AT79
AD27	VSS41	AT8
AD3	VSS42	AT82
AD34	VSS43	AT85
AD36	VSS44	AT89
AD39	VSS45	AT9
AD4	VSS46	AT92
AD6	VSS47	AT95
AD9	VSS48	AT99
AE1	VSS49	AT1
AE11	VSS50	AT11
AE20	VSS51	AT17
AE22	VSS52	AT2
AE24	VSS53	AT24
AE26	VSS54	AT29
AE34	VSS55	AT3
AE38	VSS56	AT35
AE40	VSS57	AT39
AE44	VSS58	AT4
AE8	VSS59	AT45
AF10	VSS60	AT5
AF11	VSS61	AT52
AF12	VSS62	AT55
AF13	VSS63	AT59
AF33	VSS64	AT6
AF35	VSS65	AT62
AF39	VSS66	AT66
AF7	VSS67	AT69
AG19	VSS68	AT7
AG21	VSS69	AT72
AG23	VSS70	AT75
AG25	VSS71	AT79
AG27	VSS72	AT8
AG45	VSS73	AT82
AG5	VSS74	AT85
AH2	VSS75	AT89
AH3	VSS76	AT9
AH4	VSS77	AT92
AJ20	VSS78	AT95
AJ22	VSS79	AT99
AJ24	VSS80	AT1
AJ26	VSS81	AT11
AJ28	VSS82	AT17
AJ30	VSS83	AT2
AJ32	VSS84	AT24
AJ34	VSS85	AT29
AJ36	VSS86	AT3
AJ38	VSS87	AT35
AJ40	VSS88	AT39
AJ42	VSS89	AT4
AJ44	VSS90	AT45
AJ46	VSS91	AT5
AJ48	VSS92	AT52
AJ50	VSS93	AT55
AJ52	VSS94	AT59
AJ54	VSS95	AT6
AJ56	VSS96	AT62
AJ58	VSS97	AT66
AJ60	VSS98	AT69
AJ62	VSS99	AT7
AJ64	VSS100	AT72
AJ66	VSS101	AT75
AJ68	VSS102	AT79
AJ70	VSS103	AT8
AJ72	VSS104	AT82
AJ74	VSS105	AT85
AJ76	VSS106	AT89
AJ78	VSS107	AT9
AJ80	VSS108	AT92
AJ82	VSS109	AT95
AJ84	VSS110	AT99
AJ86	VSS111	AT1
AJ88	VSS112	AT11
AJ90	VSS113	AT17
AJ92	VSS114	AT2
AJ94	VSS115	AT24
AJ96	VSS116	AT29
AJ98	VSS117	AT3
AJ100	VSS118	AT35
AJ102	VSS119	AT39
AJ104	VSS120	AT4
AJ106	VSS121	AT45
AJ108	VSS122	AT5
AJ110	VSS123	AT52
AJ112	VSS124	AT55
AJ114	VSS125	AT59
AJ116	VSS126	AT6
AJ118	VSS127	AT62
AJ120	VSS128	AT66
AJ122	VSS129	AT69
AJ124	VSS130	AT7
AJ126	VSS131	AT72
AJ128	VSS132	AT75
AJ130	VSS133	AT79
AJ132	VSS134	AT8
AJ134	VSS135	AT82
AJ136	VSS136	AT85
AJ138	VSS137	AT89
AJ140	VSS138	AT9
AJ142	VSS139	AT92
AJ144	VSS140	AT95
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AJ150	VSS143	AT11
AJ152	VSS144	AT17
AJ154	VSS145	AT2
AJ156	VSS146	AT24
AJ158	VSS147	AT29
AJ160	VSS148	AT3
AJ162	VSS149	AT35
AJ164	VSS150	AT39
AJ166	VSS151	AT4
AJ168	VSS152	AT45
AJ170	VSS153	AT5
AJ172	VSS154	AT52
AJ174	VSS155	AT55
AJ176	VSS156	AT59
AJ178	VSS157	AT6
AJ180	VSS158	AT62
AJ182	VSS159	AT66
AJ184	VSS160	AT69
AJ186	VSS161	AT7
AJ188	VSS162	AT72
AJ190	VSS163	AT75
AJ192	VSS164	AT79
AJ194	VSS165	AT8
AJ196	VSS166	AT82
AJ198	VSS167	AT85
AJ200	VSS168	AT89
AJ202	VSS169	AT9
AJ204	VSS170	AT92
AJ206	VSS171	AT95
AJ208	VSS172	AT99
AJ210	VSS173	AT1
AJ212	VSS174	AT11
AJ214	VSS175	AT17
AJ216	VSS176	AT2
AJ218	VSS177	AT24
AJ220	VSS178	AT29
AJ222	VSS179	AT3
AJ224	VSS180	AT35
AJ226	VSS181	AT39
AJ228	VSS182	AT4
AJ230	VSS183	AT45
AJ232	VSS184	AT5
AJ234	VSS185	AT52
AJ236	VSS186	AT55
AJ238	VSS187	AT59
AJ240	VSS188	AT6
AJ242	VSS189	AT62
AJ244	VSS190	AT66
AJ246	VSS191	AT69
AJ248	VSS192	AT7
AJ250	VSS193	AT72
AJ252	VSS194	AT75
AJ254	VSS195	AT79
AJ256	VSS196	AT8
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AJ260	VSS198	AT85
AJ262	VSS199	AT89
AJ264	VSS200	AT9
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AJ268	VSS202	AT95
AJ270	VSS203	AT99
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AJ274	VSS205	AT11
AJ276	VSS206	AT17
AJ278	VSS207	AT2
AJ280	VSS208	AT24
AJ282	VSS209	AT29
AJ284	VSS210	AT3
AJ286	VSS211	AT35
AJ288	VSS212	AT39
AJ290	VSS213	AT4
AJ292	VSS214	AT45
AJ294	VSS215	AT5
AJ296	VSS216	AT52
AJ298	VSS217	AT55
AJ300	VSS218	AT59
AJ302	VSS219	AT6
AJ304	VSS220	AT62
AJ306	VSS221	AT66
AJ308	VSS222	AT69
AJ310	VSS223	AT7
AJ312	VSS224	AT72
AJ314	VSS225	AT75
AJ316	VSS226	AT79
AJ318	VSS227	AT8
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AJ324	VSS230	AT89
AJ326	VSS231	AT9
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AJ336	VSS236	AT11
AJ338	VSS237	AT17
AJ340	VSS238	AT2
AJ342	VSS239	AT24
AJ344	VSS240	AT29
AJ346	VSS241	AT3
AJ348	VSS242	AT35
AJ350	VSS243	AT39
AJ352	VSS244	AT4
AJ354	VSS245	AT45
AJ356	VSS246	AT5
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AJ360	VSS248	AT55
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AJ364	VSS250	AT6
AJ366	VSS251	AT62
AJ368	VSS252	AT66
AJ370	VSS253	AT69
AJ372	VSS254	AT7
AJ374	VSS255	AT72
AJ376	VSS256	AT75
AJ378	VSS257	AT79
AJ380	VSS258	AT8
AJ382	VSS259	AT82
AJ384	VSS260	AT85
AJ386	VSS261	AT89
AJ388	VSS262	AT9
AJ390	VSS263	AT92
AJ392	VSS264	AT95
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AJ396	VSS266	AT1
AJ398	VSS267	AT11
AJ400	VSS268	AT17
AJ402	VSS269	AT2
AJ404	VSS270	AT24
AJ406	VSS271	AT29
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AJ410	VSS273	AT35
AJ412	VSS274	AT39
AJ414	VSS275	AT4
AJ416	VSS276	AT45
AJ418	VSS277	AT5
AJ420	VSS278	AT52
AJ422	VSS279	AT55
AJ424	VSS280	AT59
AJ426	VSS281	AT6
AJ428	VSS282	AT62
AJ430	VSS283	AT66
AJ432	VSS284	AT69
AJ434	VSS285	AT7
AJ436	VSS286	AT72
AJ438	VSS287	AT75
AJ440	VSS288	AT79
AJ442	VSS289	AT8
AJ444	VSS290	AT82
AJ446	VSS291	AT85
AJ448	VSS292	AT89
AJ450	VSS293	AT9
AJ452	VSS294	AT92
AJ454	VSS295	AT95
AJ456	VSS296	AT99
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AJ462	VSS299	AT17
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AJ478	VSS307	AT45
AJ480	VSS308	AT5
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AJ486	VSS311	AT59
AJ488	VSS312	AT6
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AJ504	VSS320	AT8
AJ506	VSS321	AT82
AJ508	VSS322	AT85
AJ510	VSS323	AT89
AJ512	VSS324	AT9
AJ514	VSS325	AT92
AJ516	VSS326	AT95
AJ518	VSS327	AT99
AJ520	VSS328	AT1
AJ522	VSS329	AT11
AJ524	VSS330	AT17
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AJ530	VSS333	AT29
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AJ536	VSS336	AT39
AJ538	VSS337	AT4
AJ540	VSS338	AT45
AJ542	VSS339	AT5
AJ544	VSS340	AT52
AJ546	VSS341	AT55
AJ548	VSS342	AT59
AJ550	VSS343	AT6
AJ552	VSS344	AT62
AJ554	VSS345	AT66
AJ556	VSS346	AT69
AJ558	VSS347	AT7
AJ560	VSS348	AT72
AJ562	VSS349	AT75
AJ564	VSS350	AT79
AJ566	VSS351	AT8
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AJ570	VSS353	AT85
AJ572	VSS354	AT89
AJ574	VSS355	AT9
AJ576	VSS356	AT92
AJ578	VSS357	AT95
AJ580	VSS358	AT99
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AJ596	VSS366	AT35
AJ598	VSS367	AT39
AJ600	VSS368	AT4
AJ602	VSS369	AT45
AJ604	VSS370	AT5
AJ606	VSS371	AT52
AJ608	VSS372	AT55
AJ610	VSS373	AT59
AJ612	VSS374	AT6
AJ614	VSS375	AT62
AJ616	VSS376	AT66
AJ618	VSS377	AT69
AJ620	VSS378	AT7
AJ622	VSS379	AT72
AJ624	VSS380	AT75
AJ626	VSS381	AT79
AJ628	VSS382	AT8
AJ630	VSS383	AT82
AJ632	VSS384	AT85
AJ634	VSS385	AT89
AJ636	VSS386	AT9
AJ638	VSS387	AT92
AJ640	VSS388	AT95
AJ642	VSS389	AT99
AJ644	VSS390	AT1
AJ646	VSS391	AT11
AJ648	VSS392	AT17
AJ650	VSS393	AT2
AJ652	VSS394	AT24
AJ654	VSS395	AT29
AJ656	VSS396	AT3
AJ658	VSS397	AT35
AJ660	VSS398	AT39
AJ662	VSS399	AT4
AJ664	VSS400	AT45
AJ666	VSS401	AT5
AJ668	VSS402	AT52
AJ670	VSS403	AT55
AJ672	VSS404	AT59
AJ674	VSS405	AT6
AJ676	VSS406	AT62
AJ678	VSS407	AT66
AJ680	VSS408	AT69
AJ682	VSS409	AT7



XMM3A
DDR2_DIMM_240P

XMM3 COLOR: BLUE

XMM4A
DDR2_DIMM_240P

XMM4 FURTHEST FROM CPU
XMM4 COLOR: BLACK

XMM3B
DDR2_DIMM_240P

Note:
Change power source to +3P3V_CL for iAMT support

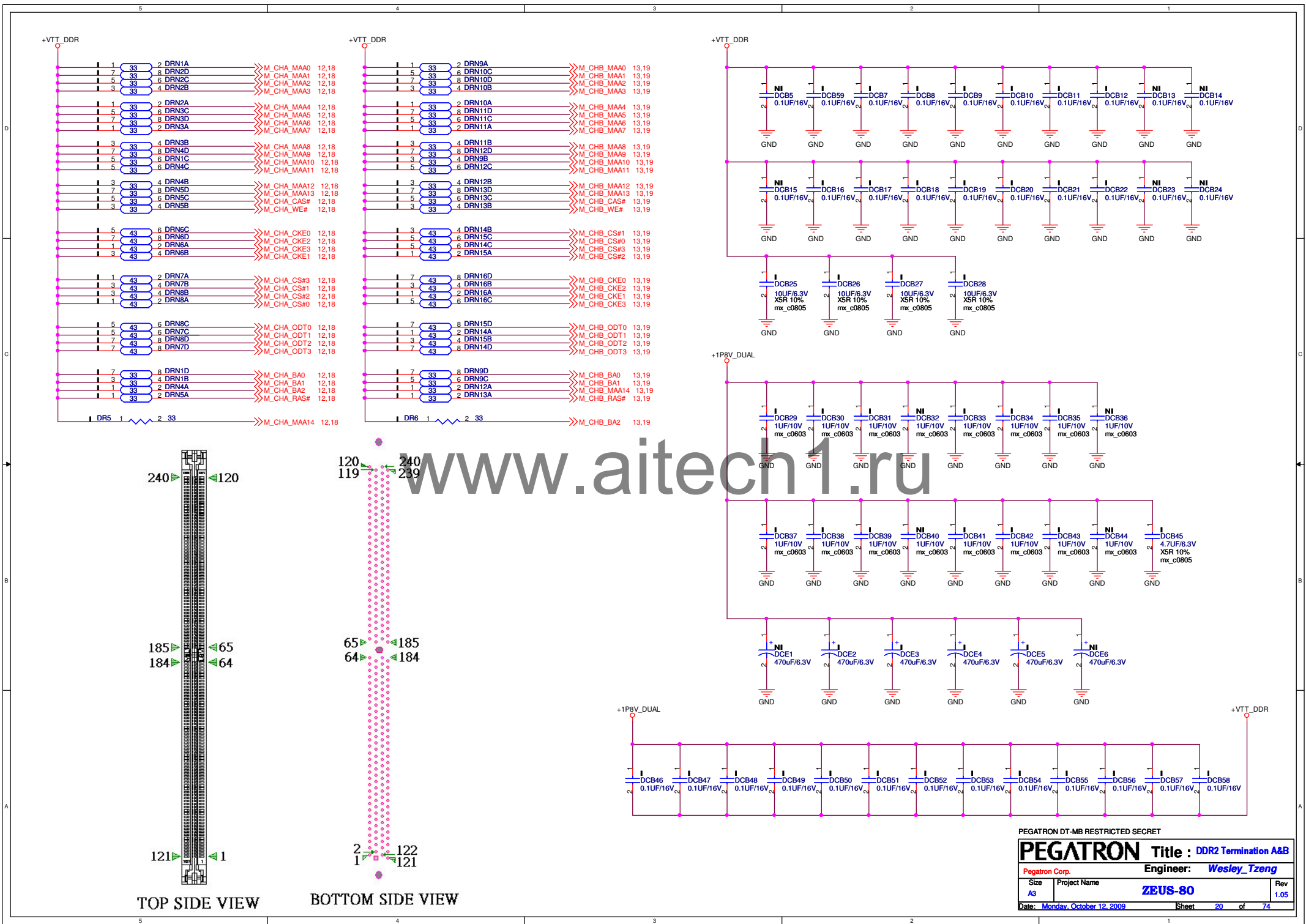
XMM4B
DDR2_DIMM_240P

Note:
Change power source to +3P3V_CL for iAMT support

PEGATRON DT-MB RESTRICTED SECRET

PEGATRON Title : DDR2 CHANNEL B
Pegatron Corp. Engineer: Wesley_Tzeng

Size	Project Name	Rev
A3	ZEUS-80	1.05
Date: Monday, October 12, 2009	Sheet 19 of 74	



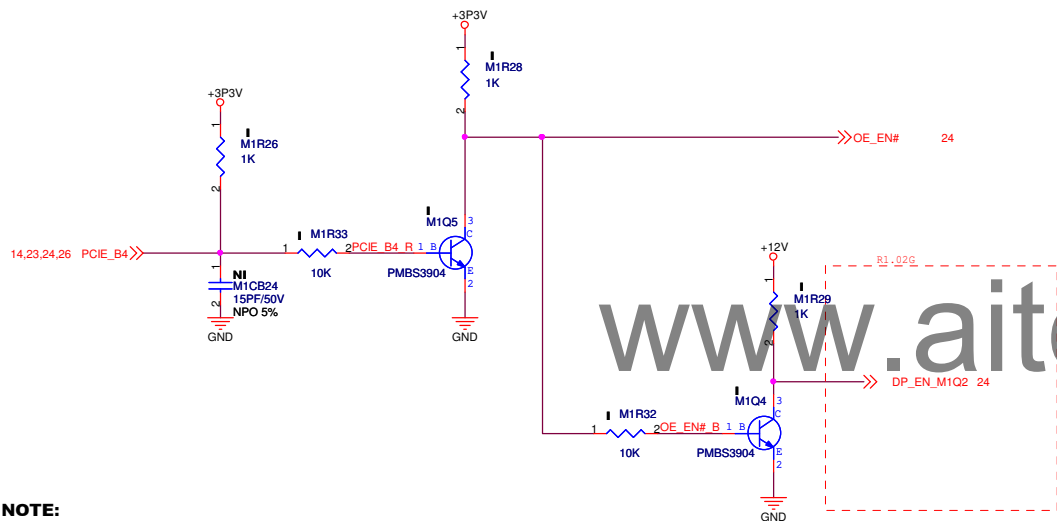
TOP SIDE VIEW

BOTTOM SIDE VIEW

PEGATRON DT-MB RESTRICTED SECRET

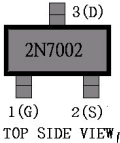
PEGATRON		Title : <i>DDR2 Termination A&B</i>	
Pegatron Corp.		Engineer: <i>Wesley_Tzeng</i>	
Size A3	Project Name ZEUS-80		Rev 1.05
Date: <i>Monday, October 12, 2009</i>		Sheet <i>20</i> of <i>74</i>	

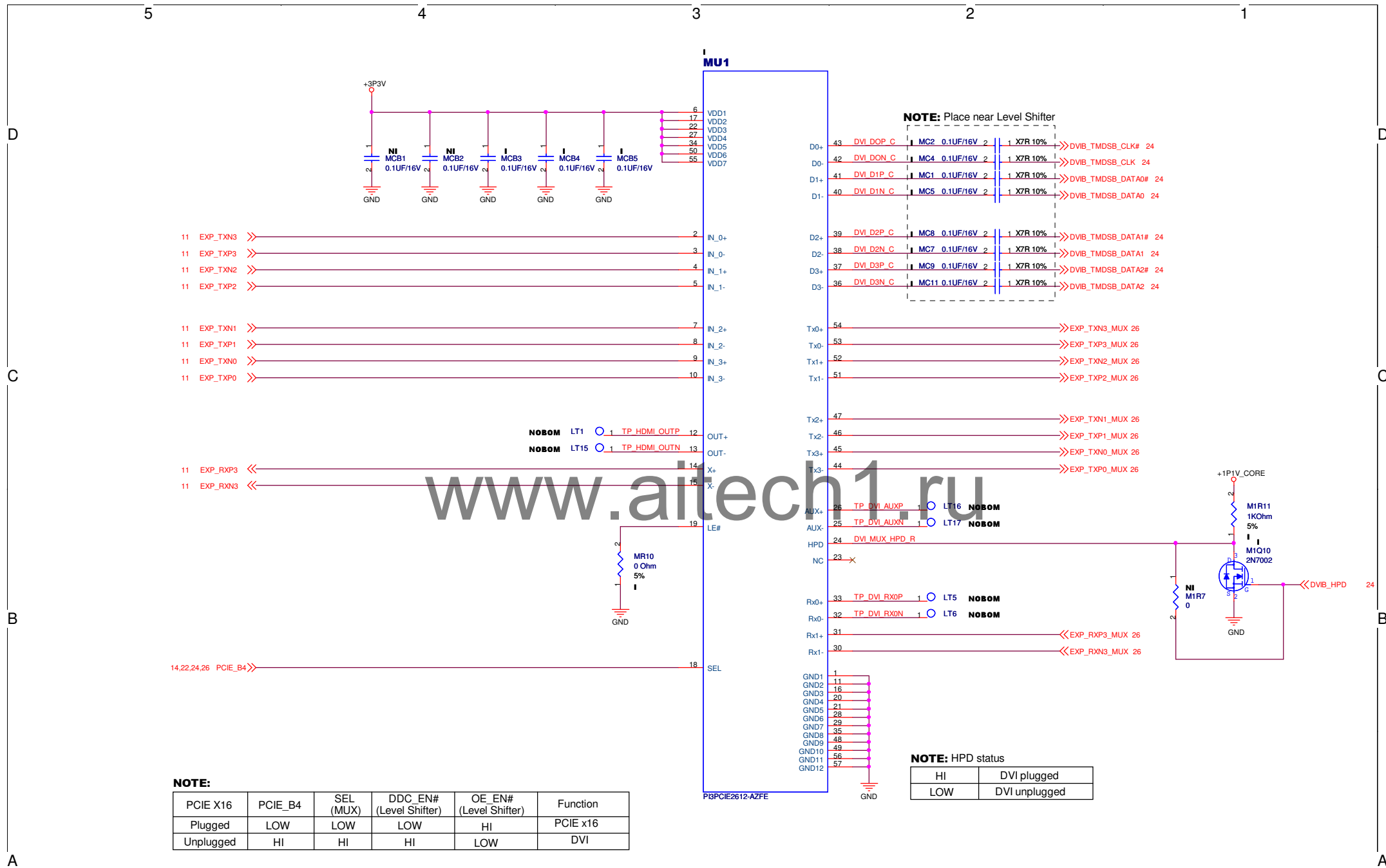
Digital Port Switch Control Logic

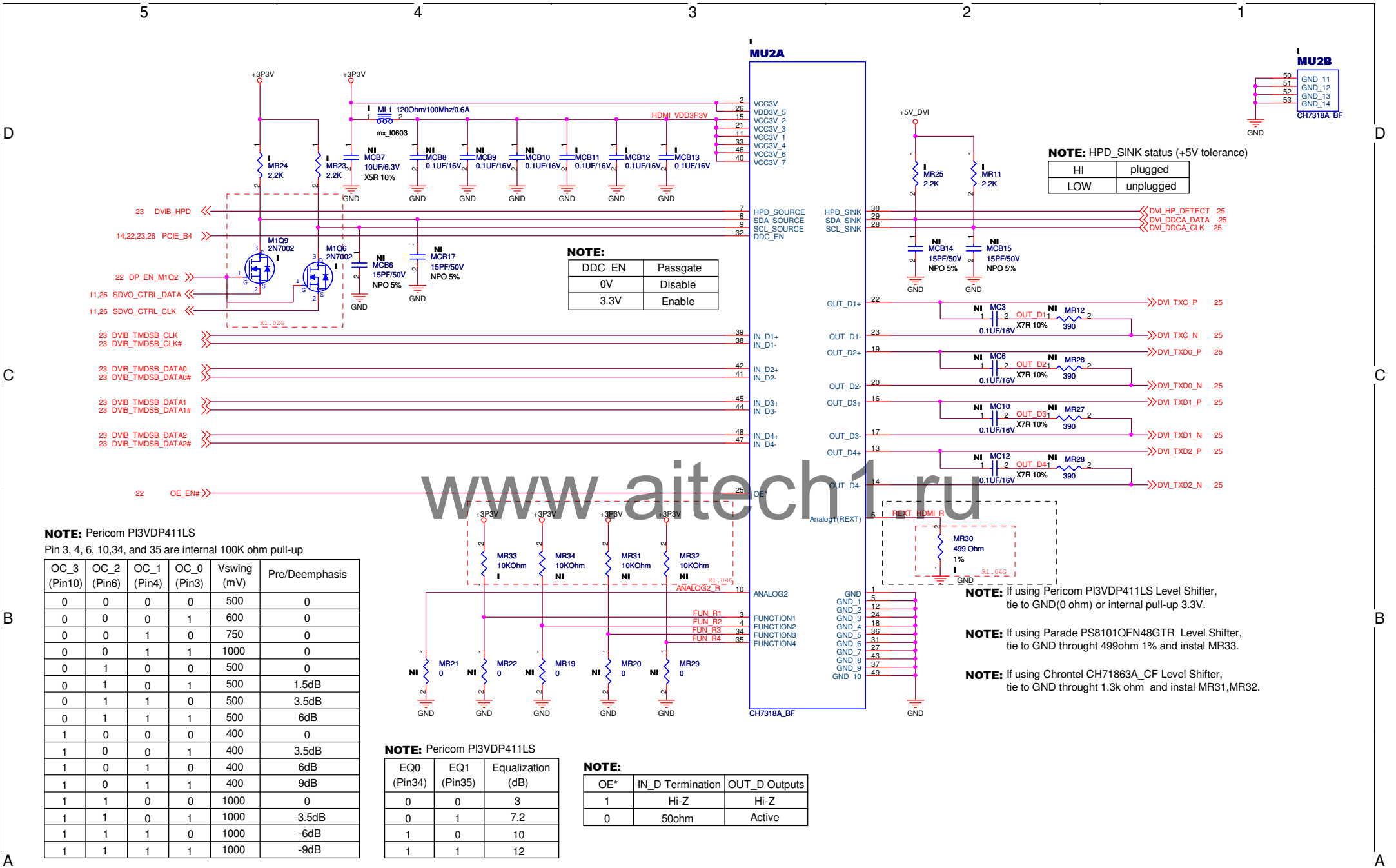


NOTE:

PCIE X16	PCIE_B4	SEL (MUX)	DDC_EN# (Level Shifter)	OE_EN# (Level Shifter)	Function
Plugged	LOW	LOW	LOW	HI	PCIE x16
Unplugged	HI	HI	HI	LOW	DVI



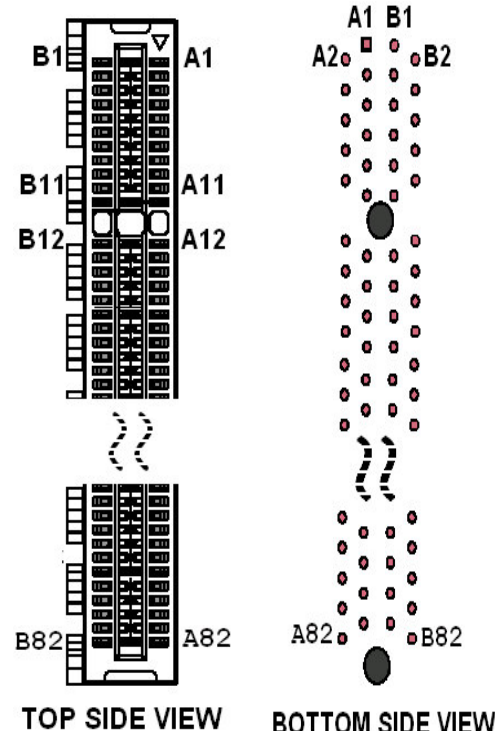
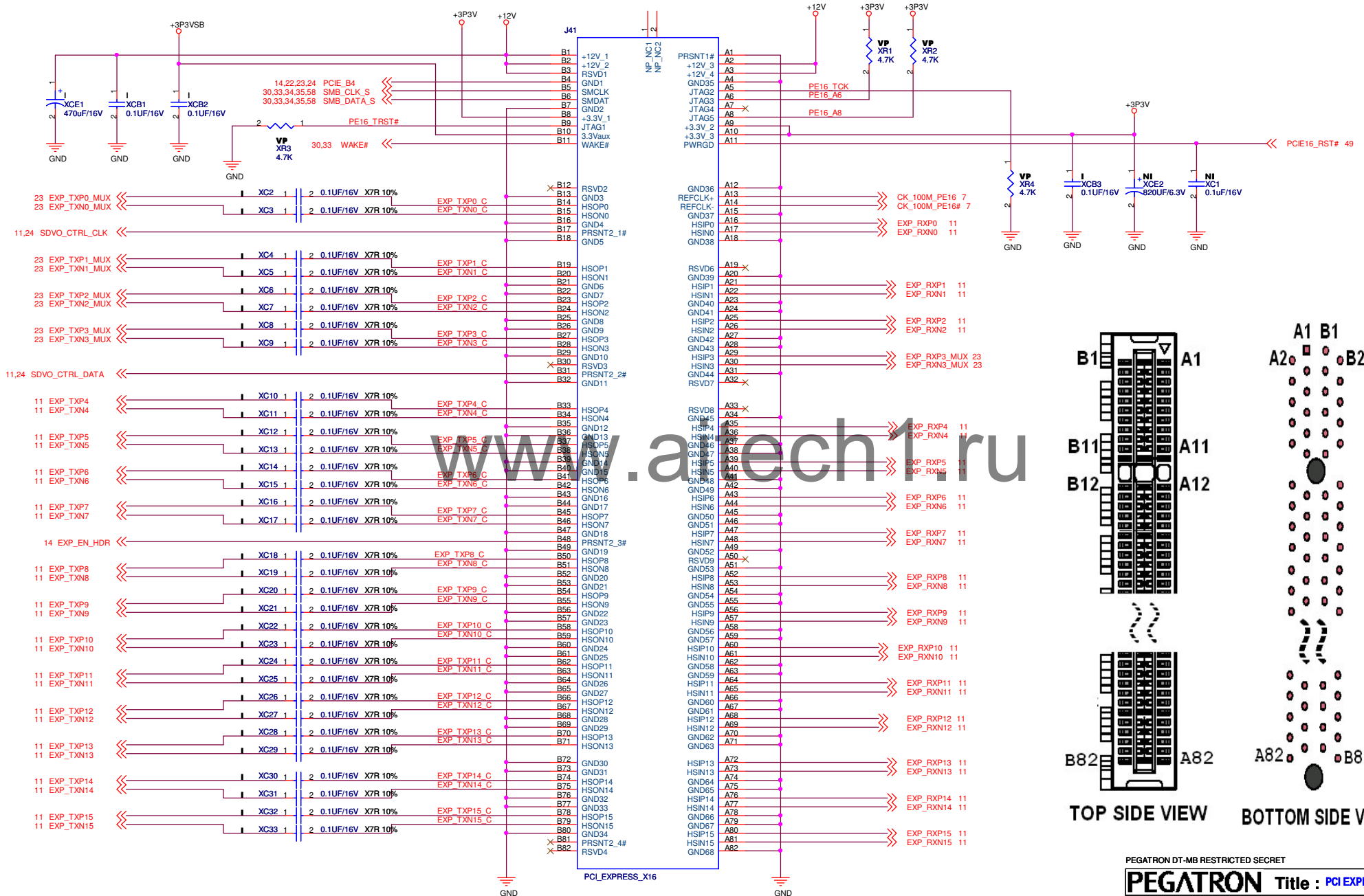


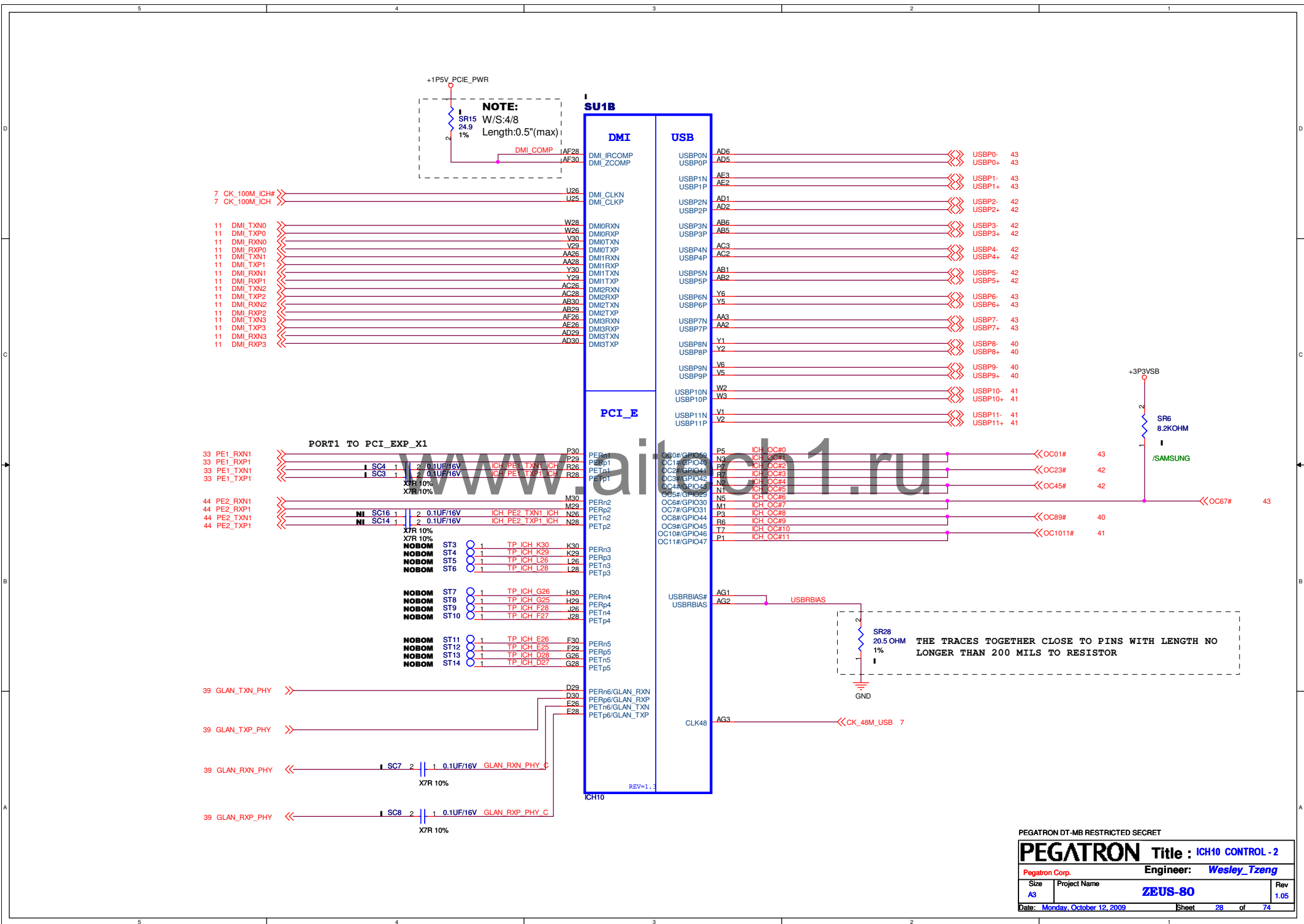


PEGATRON DT-MB RESTRICTED SECRET

PEGATRON		Title : DVI LEVEL SHIFTER	
Pegatron Corp.		Engineer: Wesley_Tzeng	
Size	Project Name	Rev	
A3	ZEUS-80	1.05	
Date: Monday, October 12, 2009		Sheet	24 of 74

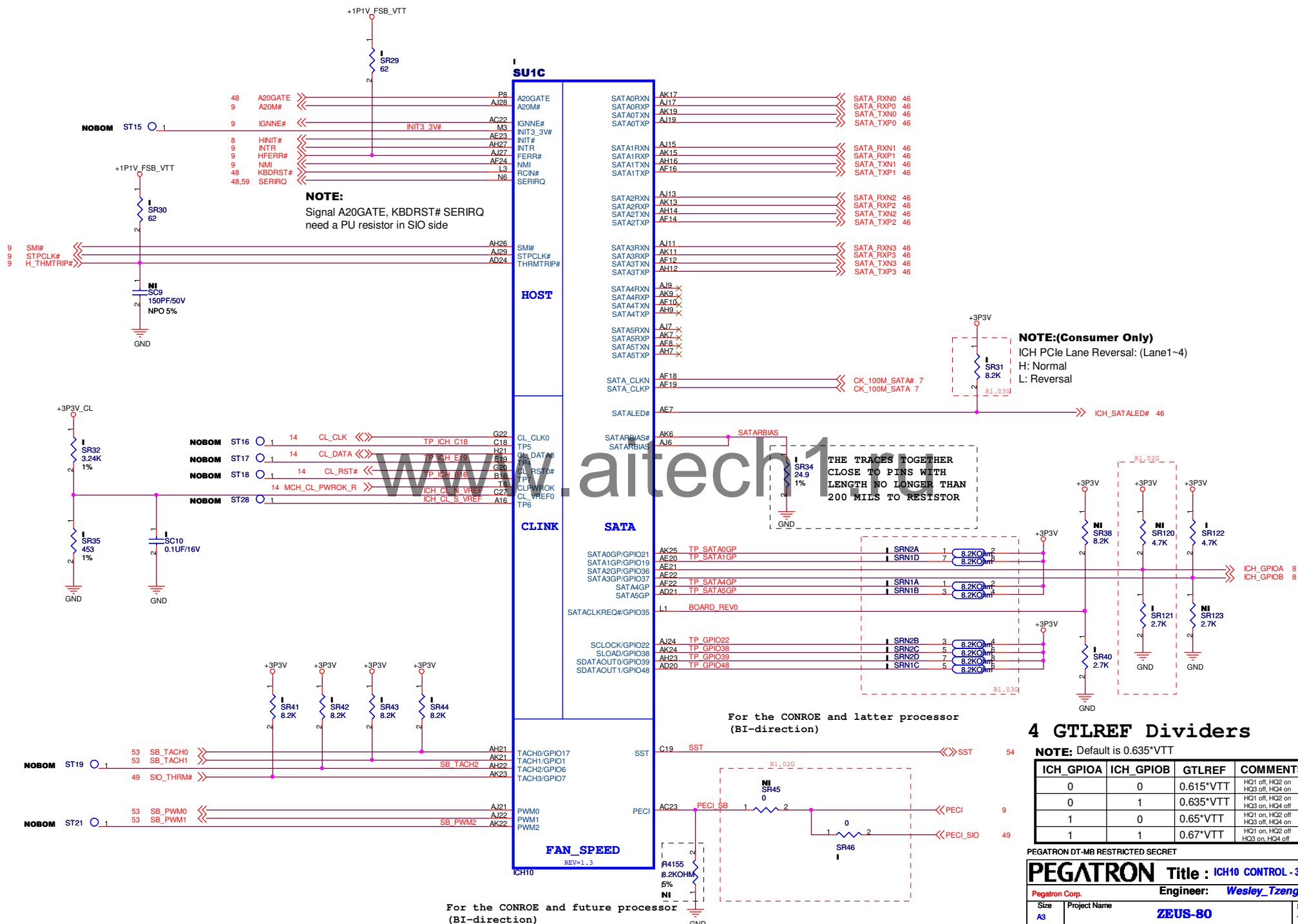
PCI EXPRESS X16 Graphics Card Slot





PEGATRON DT-MB RESTRICTED SECRET

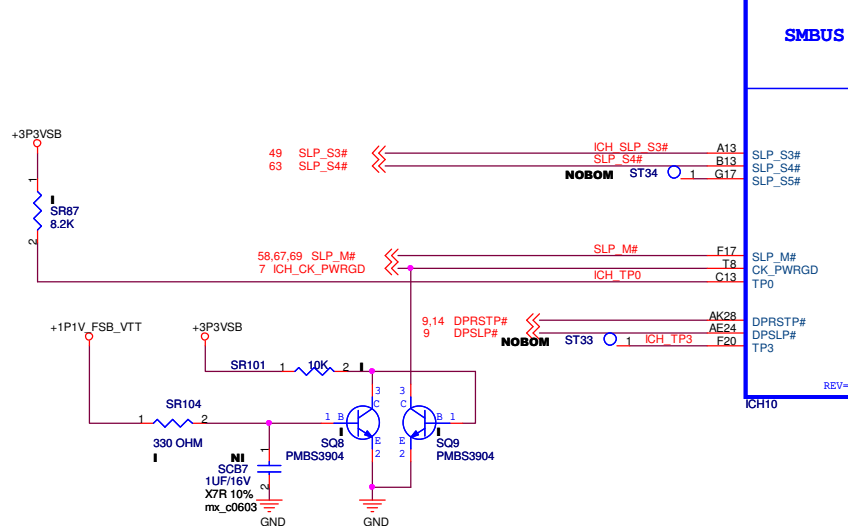
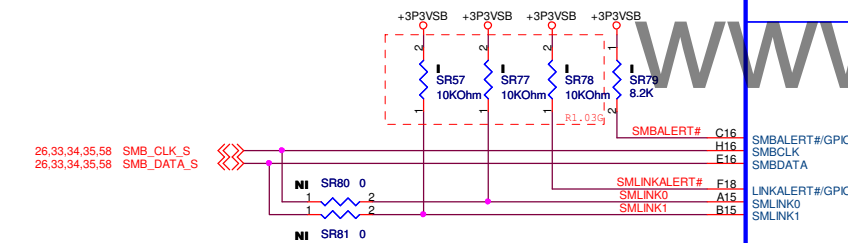
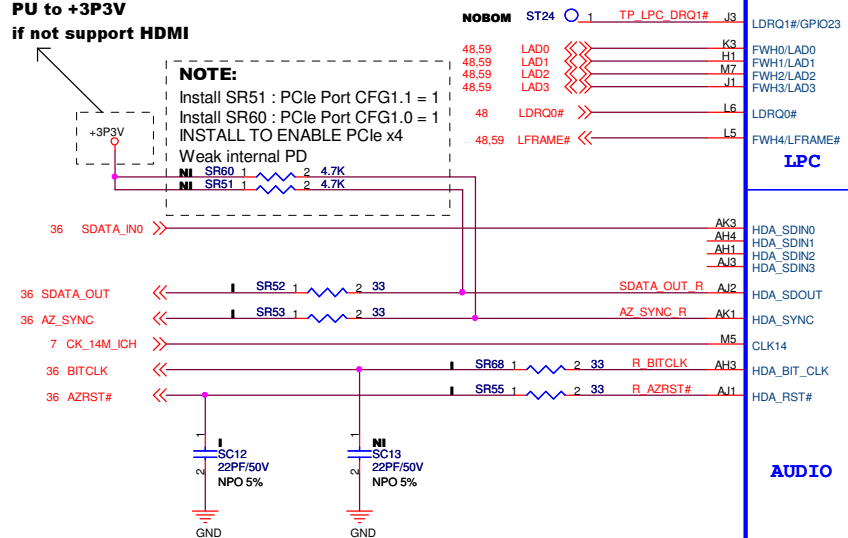
PEGATRON		Title : ICH10 CONTROL -2	
Pegatron Corp.		Engineer: Wesley_Tzeng	
Size A3	Project Name ZEUS-80	Rev 1.05	
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SDATA_IN0	HDA_LINK HEADER(P76)
SDATA_IN1	HDA_LINK HEADER(P76)
SDATA_IN2	Audio Codec
SDATA_IN3	Eaglelake GMCH

	Consumer		Coporate	
SR51	NI	I	I	NI
SR60	NI	I	NI	NI
	four x1 PCIe	one x4 PCIe	Danbury Enable	Danbury Disable

NOTE:
Install SR51: PCIe Port CFG1.1 = 1
Install SR60: PCIe Port CFG1.0 = 1
INSTALL TO ENABLE PCIe x4



LDRQ1#/GPIO23
FWH0/LAD0
FWH1/LAD1
FWH2/LAD2
FWH3/LAD3
LDRQ0#
FWH4/LFRAME#
LPC

SMBALERT#/GPIQ
SMBCLK
SMBDATA

LINKALERT#/GPIQ
SMLINK0
SMLINK1

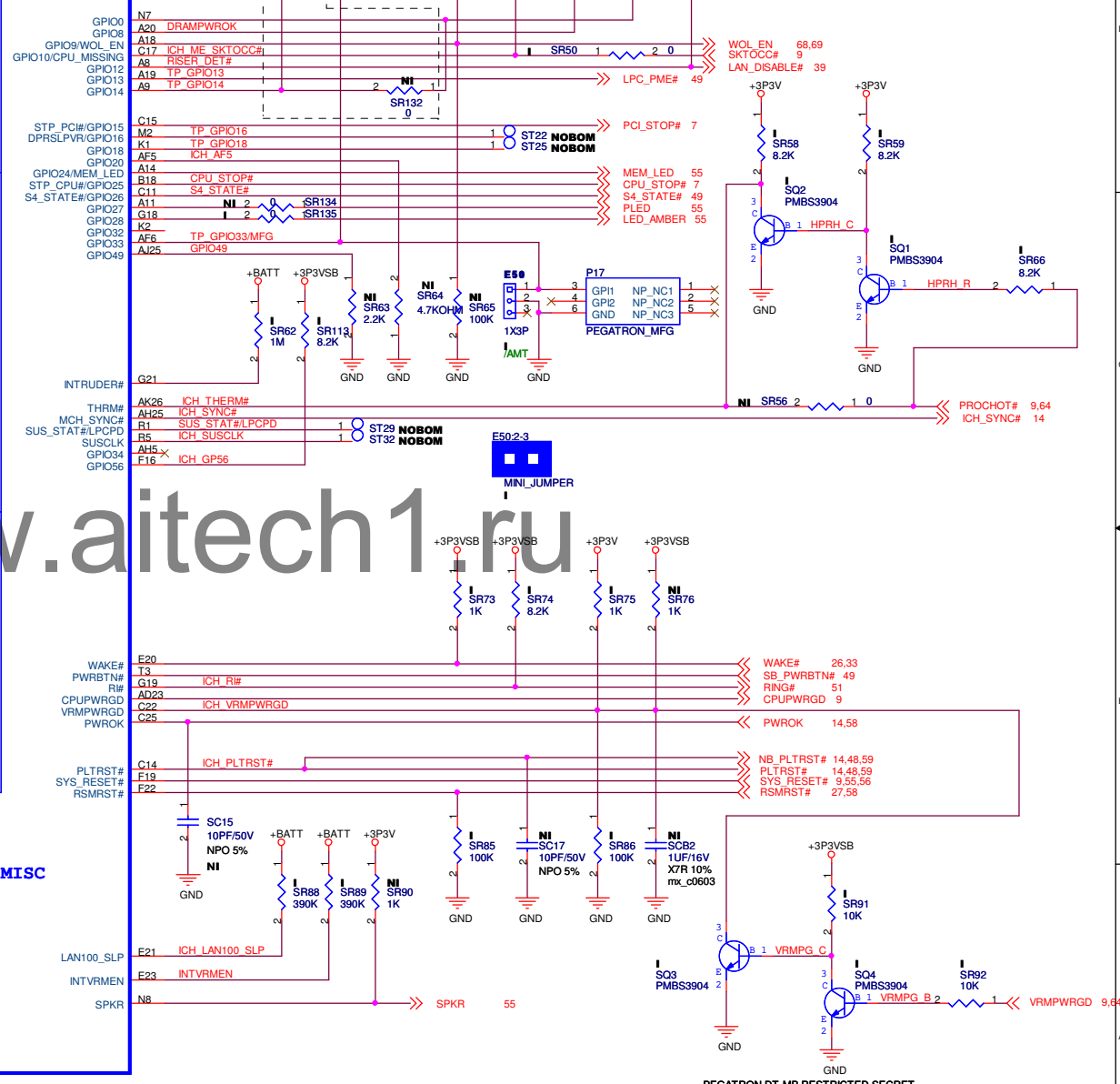
SMBUS

SLP_S3#
SLP_S4#
SLP_S5#

SLP_M#
CK_PWRGD
TP0

DPRSTP#
DPSLP#
TP3

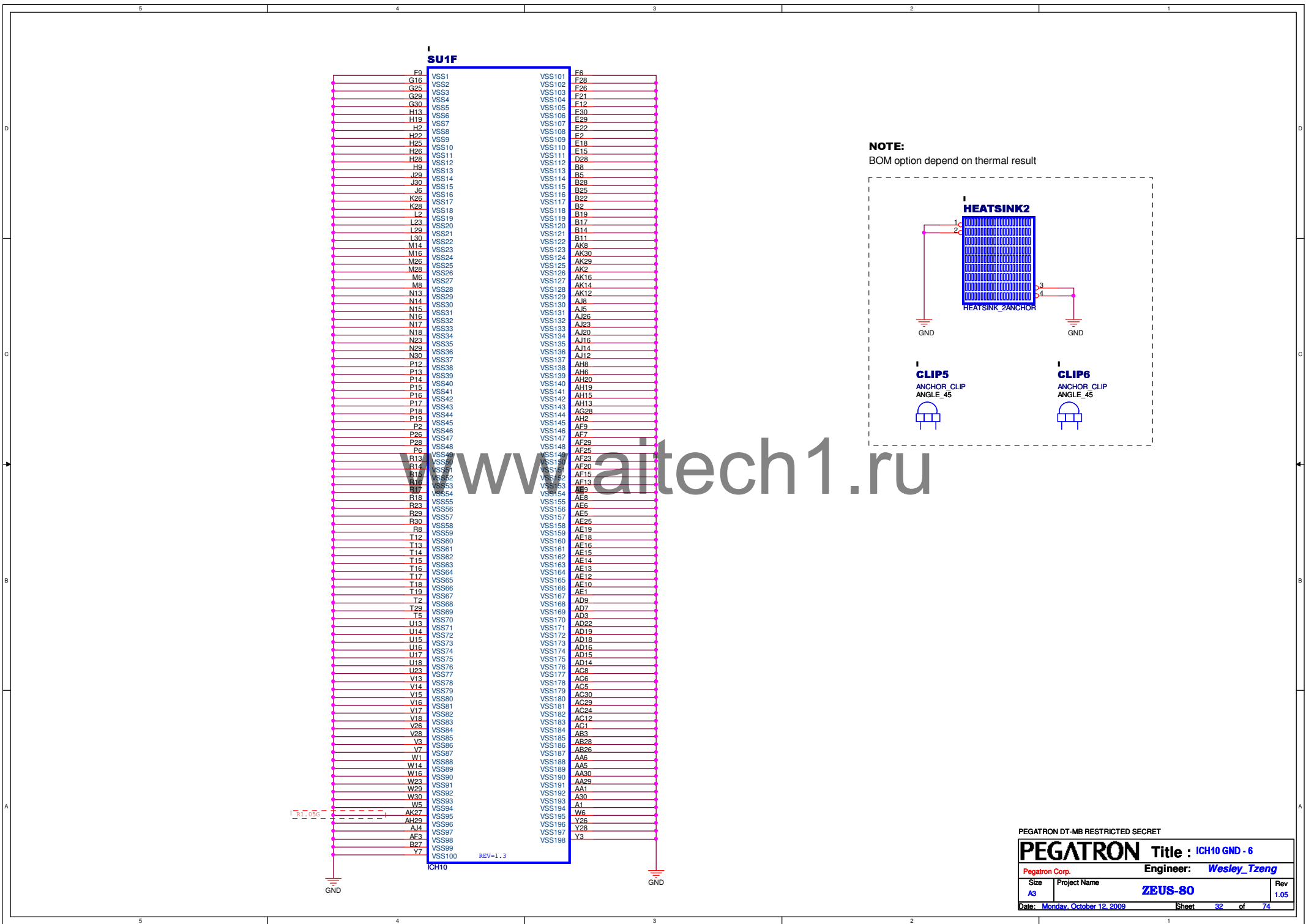
If fan control is implemented in SB,
then install SR132, NI SR133,
remove PECI_REQUEST# net.



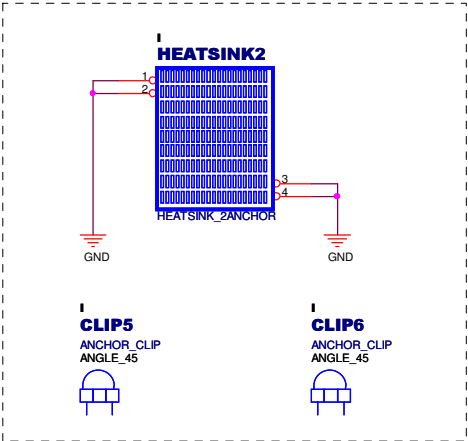
PEGATRON DT-MB RESTRICTED SECRET

PEGATRON Title : ICH10 CONTROL - 4

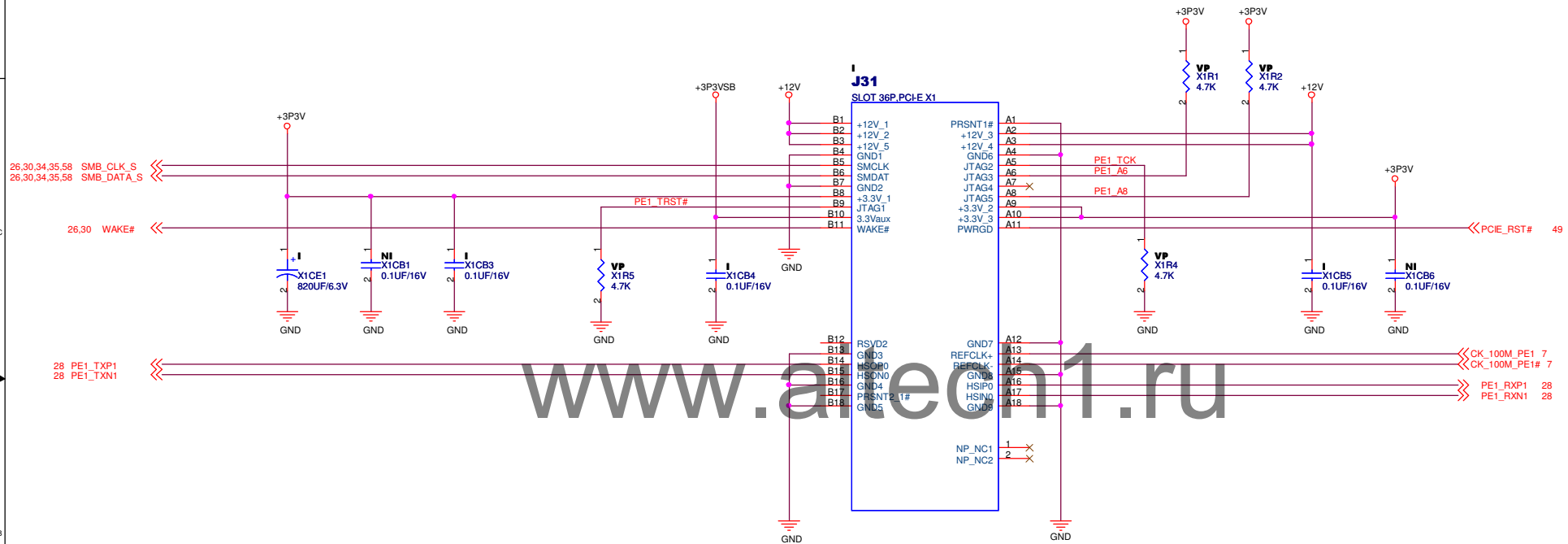
Pegatron Corp.		Engineer:	Wesley_Tzeng
Size A3	Project Name	ZEUS-80	Rev 1.05
Date:	Monday, October 12, 2009	Sheet	30 of 74



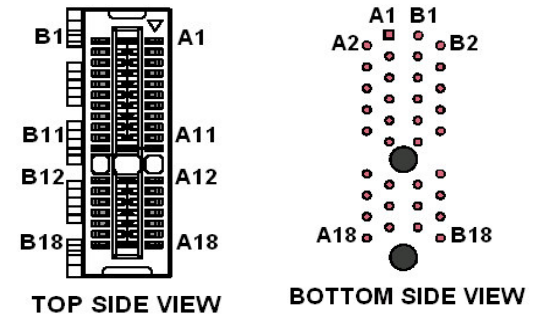
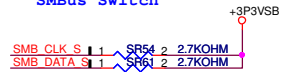
NOTE:
BOM option depend on thermal result



PCI Express x1 SLOT1

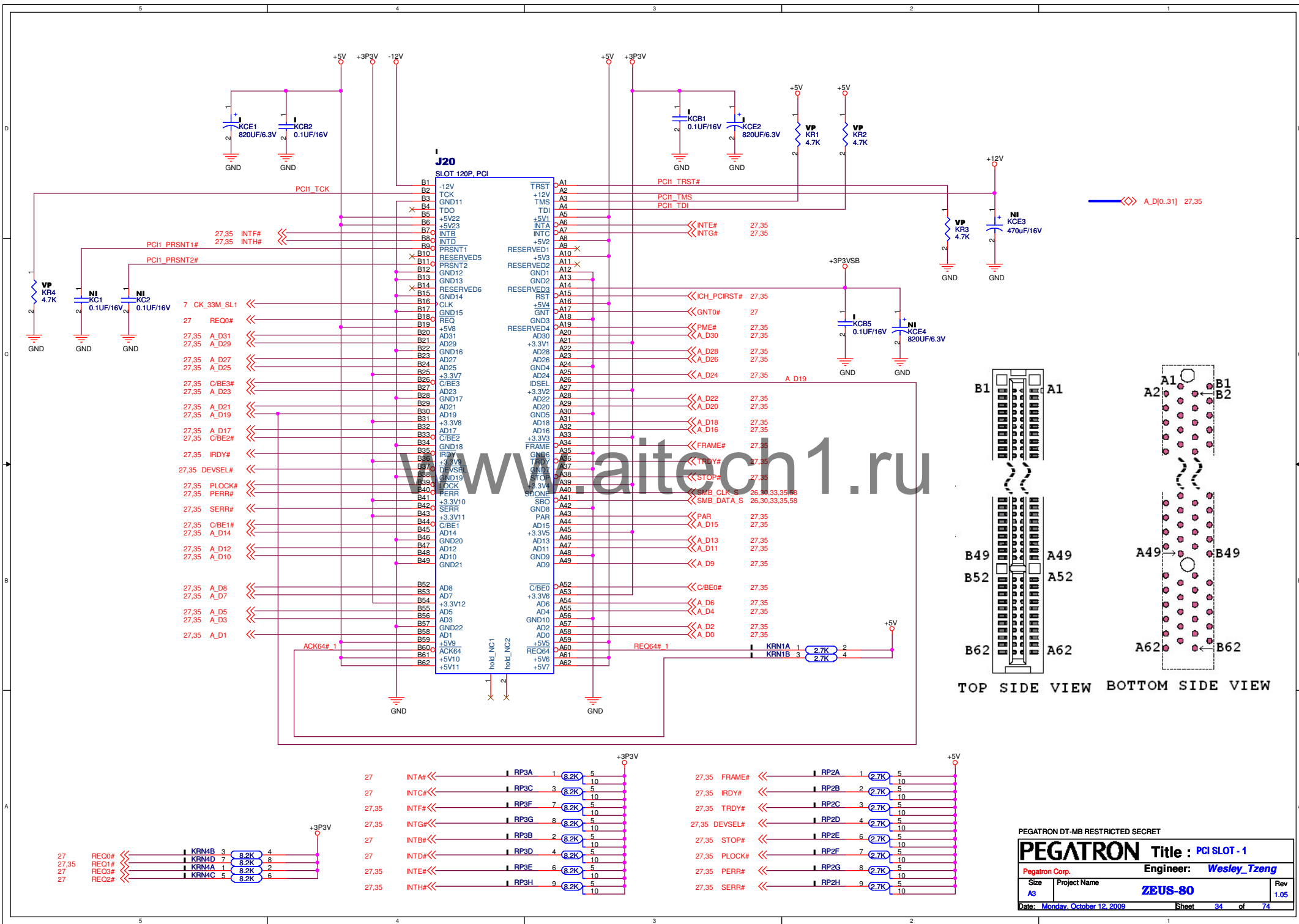


SMBus Switch



PEGATRON DT-MB RESTRICTED SECRET

PEGATRON		Title : PCI EXPRESS X1	
Pegatron Corp.		Engineer: Wesley_Tzeng	
Size A3	Project Name ZEUS-80	Rev 1.05	
Date: Monday, October 12, 2009		Sheet 33 of 74	



PEGATRON DT-MB RESTRICTED SECRET

PEGATRON		Title : <u>PCI SLOT - 1</u>	
Pegatron Corp.		Engineer: <u>Wesley_Tzeng</u>	
Size <u>A3</u>	Project Name <u>ZEUS-80</u>	Rev <u>1.05</u>	
Date: <u>Monday, October 12, 2009</u>		Sheet <u>34</u> of <u>74</u>	

Figure 1 consists of two schematic diagrams, (a) and (b), illustrating the experimental setup. Diagram (a) is a top view of the microfluidic chip, showing a central array of microfluidic channels (A2 to B2) flanked by inlet (A1) and outlet (B1) ports. The channels are represented by a grid of small circles, and the inlet/outlet ports are larger circles. Diagram (b) is a side view of the microfluidic chip, showing the inlet (A1), outlet (B1), and the array of microfluidic channels (A2 to B2) from a different perspective. The channels are represented by a grid of small circles, and the inlet/outlet ports are larger circles. The diagrams are labeled with A1, B1, A2, B2, A49, B49, A52, B52, A62, and B62.

TOP SIDE VIEW BOTTOM SIDE VIEW

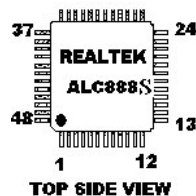
PEGATRON DT-MB RESTRICTED SECRET

PEGATRON Title : PCI SLOT - 2

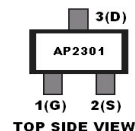
Engineer: *Wesley_Tzeng*

Size	Project Name	Rev
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A3	ZEUS-80	1.05
Date: Monday, October 12, 2009		Sheet 35 of 74



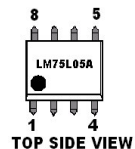
Please note:
AZ_BITCLK need add
a serial res(22 ohm)
near SB side



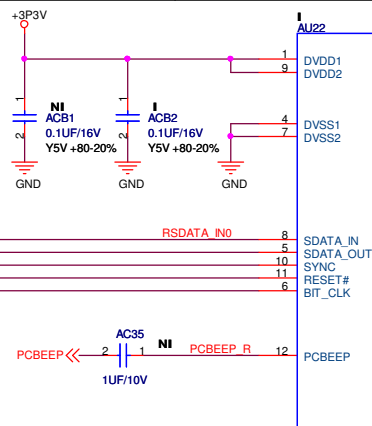
30 SDATA_IN0
30 SDATA_OUT
30 AZ_SYNC
30 AZRST#
30 BITCLK

Provision AR23 for ALC888S-VC codec

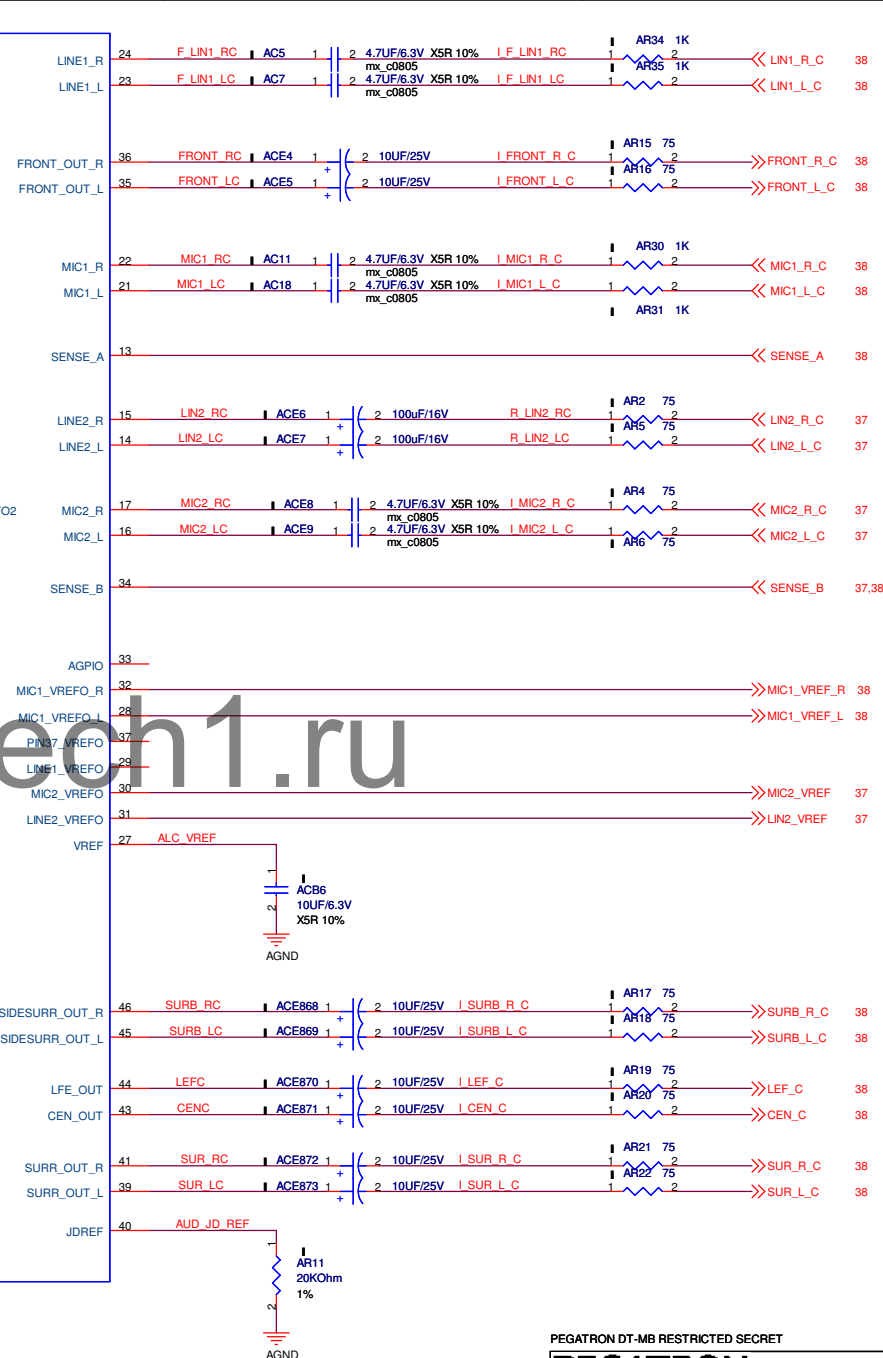
Digital Region



PLACE NEAR front audio CODEC FOR EMI

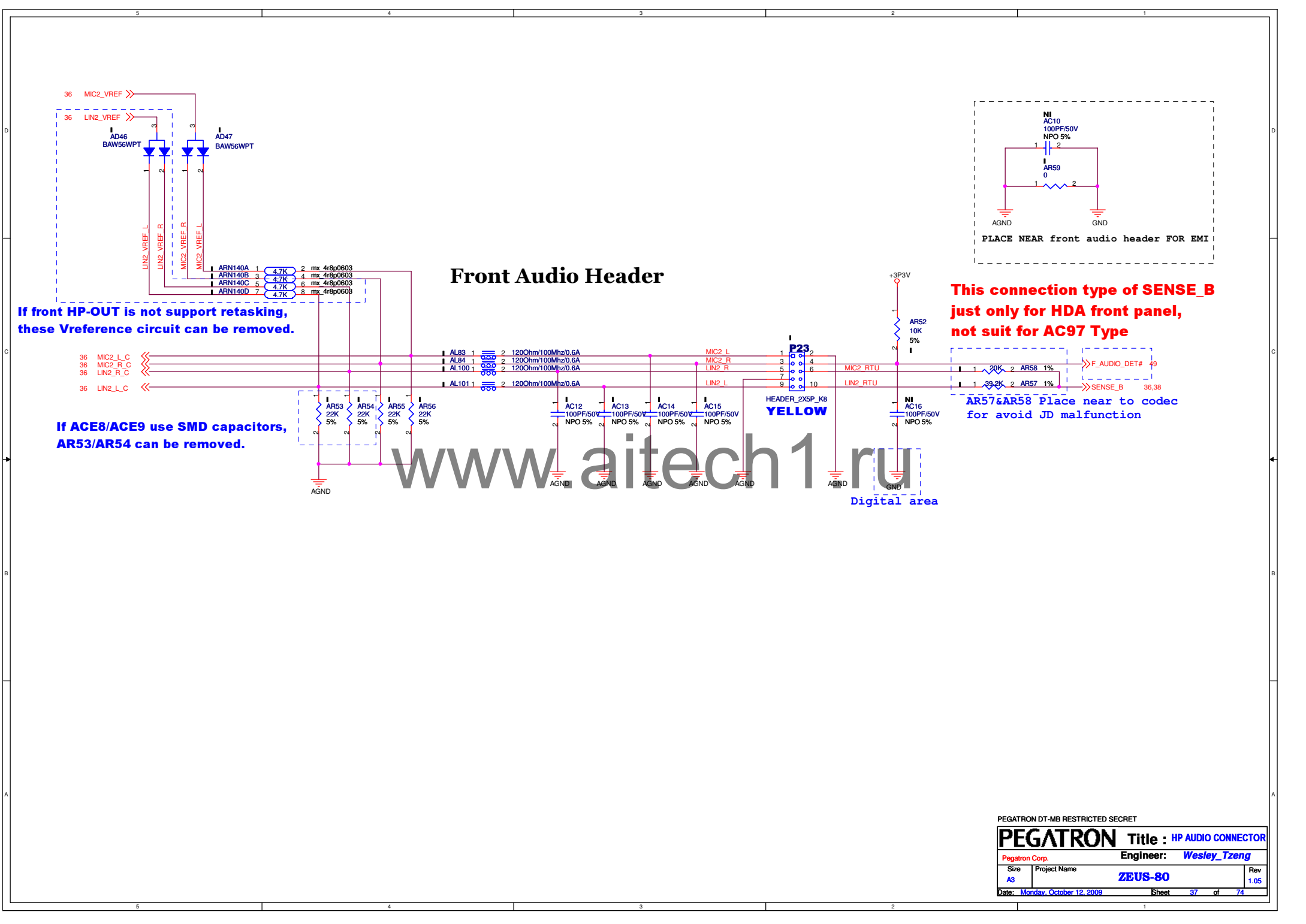


ALC888S Rev. A



PEGATRON DT-MB RESTRICTED SECRET

PEGATRON		Title : REALTEK ALC888S-VC	
Pegatron Corp.		Engineer: Wesley_Tzeng	
Size A3	Project Name ZEUS-80		Rev 1.05
Date: Monday, October 12, 2009		Sheet 36 of 74	



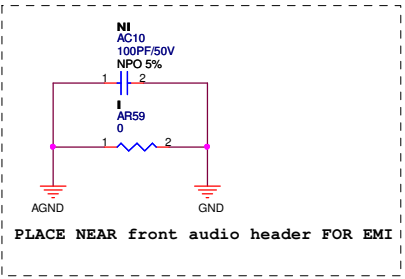
Front Audio Header

If front HP-OUT is not support retasking, these Vreference circuit can be removed.

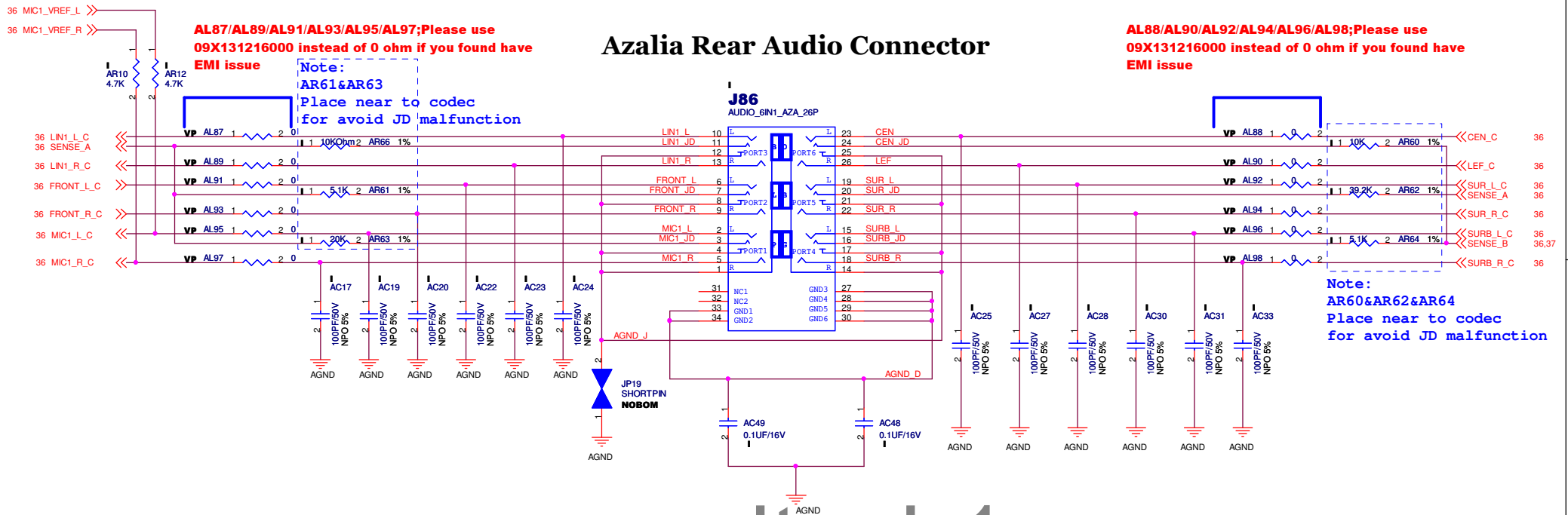
If ACE8/ACE9 use SMD capacitors, AR53/AR54 can be removed.

This connection type of SENSE_B just only for HDA front panel, not suit for AC97 Type

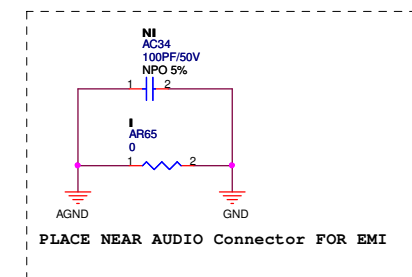
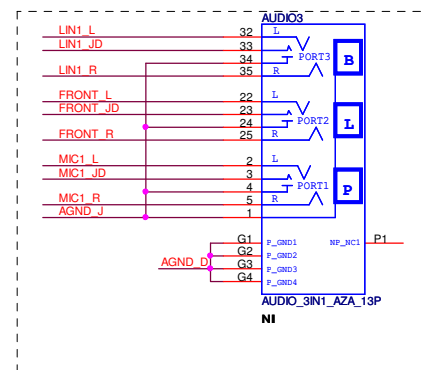
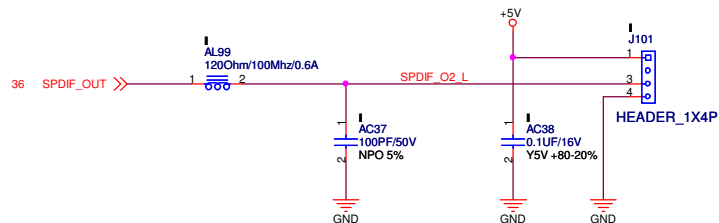
AR57&AR58 Place near to codec for avoid JD malfunction



Azalia Rear Audio Connector

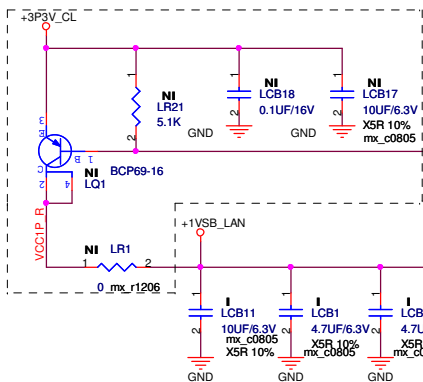


SPDIF OUT CONNECTOR

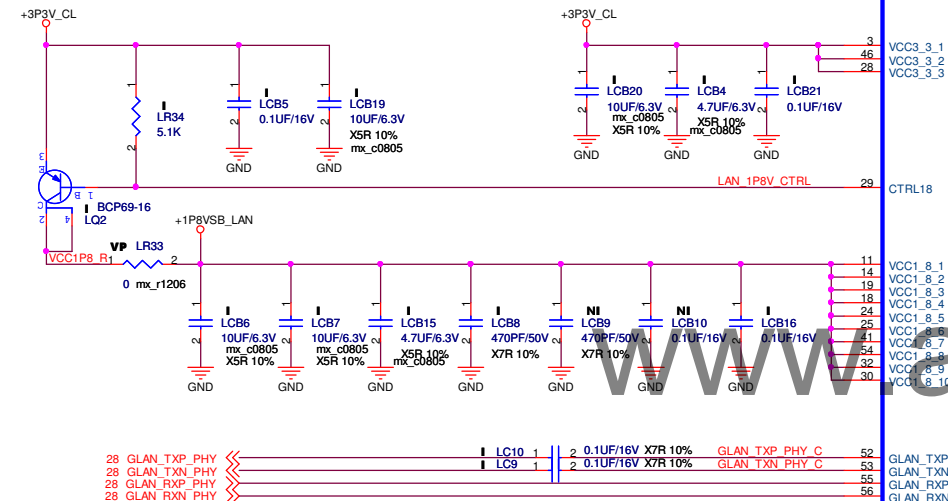


PEGATRON DT-MB RESTRICTED SECRET

PEGATRON		Title : REAR AUDIO CONNECTOR	
Pegatron Corp.		Engineer: Wesley_Tzeng	
Size A3	Project Name ZEUS-80	Rev 1.05	
Date: Monday, October 12, 2009		Sheet 38 of 74	



NOTE:
Power delivery using
external LVR for 1.0V

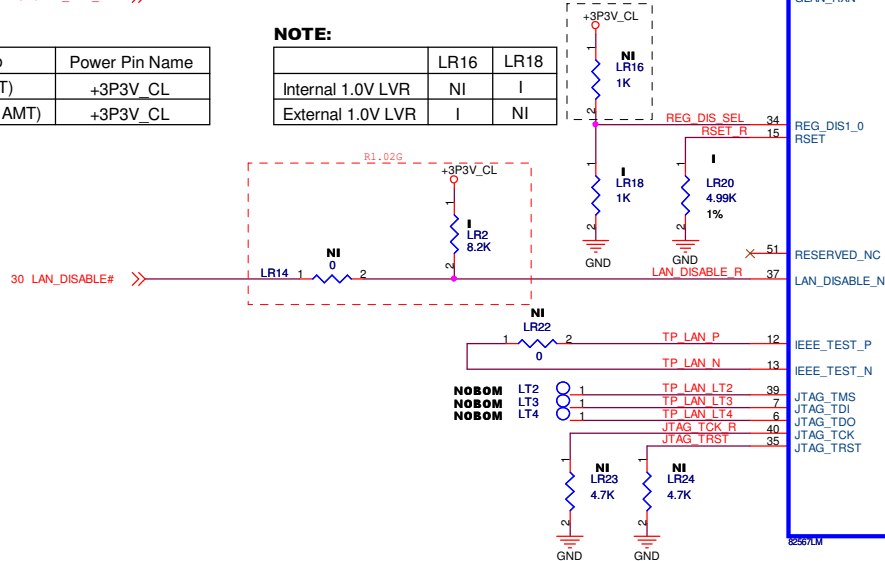


NOTE:

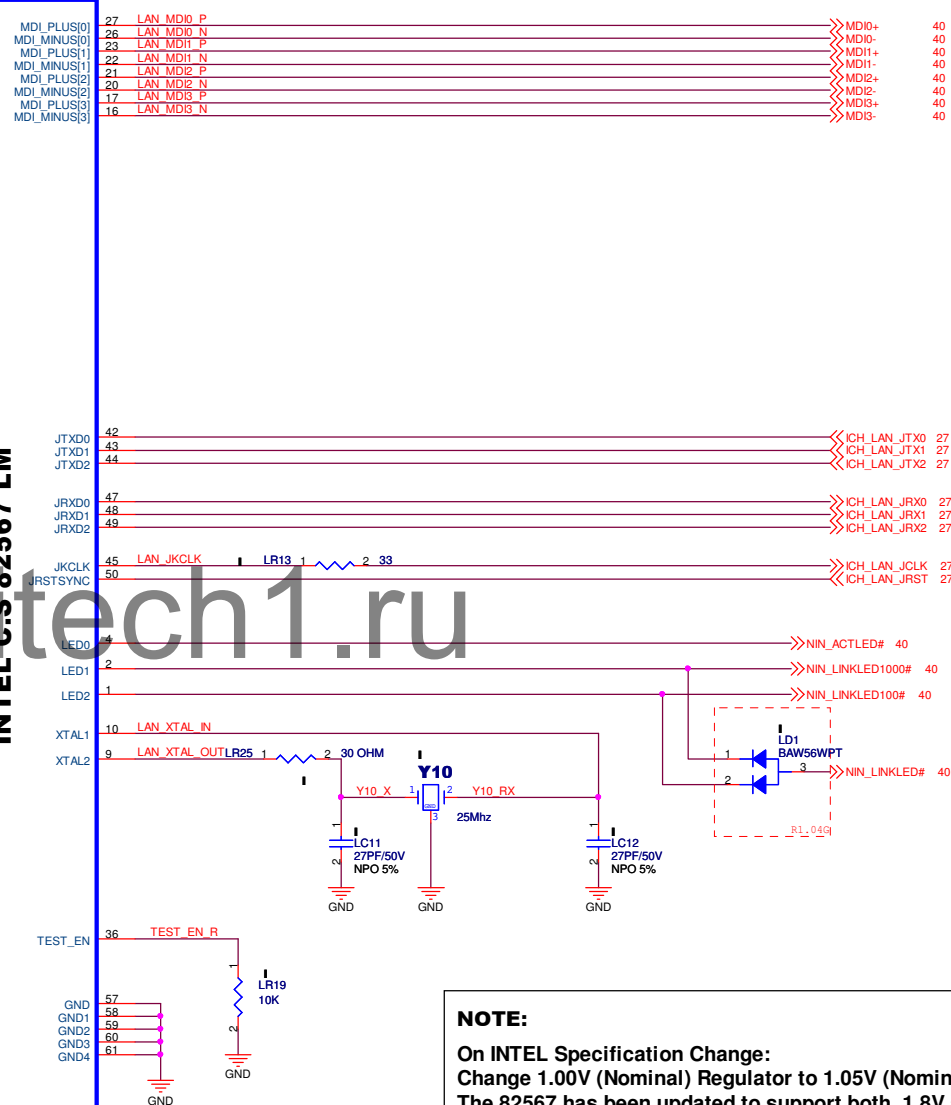
LAN Chip	Power Pin Name
82567LM(AMT)	+3P3V_CL
82567LF(non AMT)	+3P3V_CL

NOTE:

	LR16	LR18
Internal 1.0V LVR	NI	I
External 1.0V LVR	I	NI



INTEL C-S 82567 LM



NOTE:

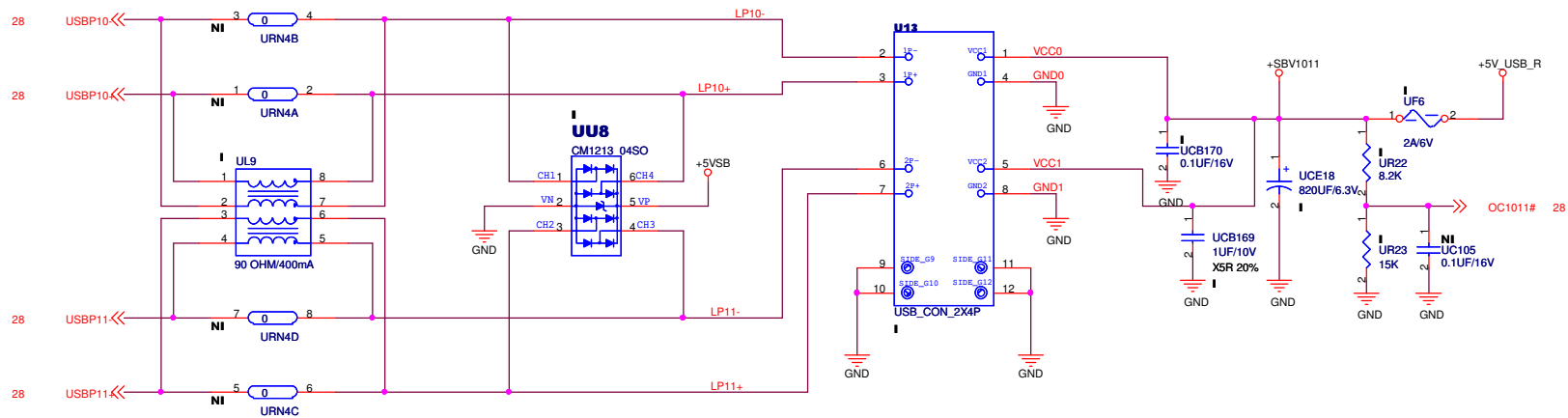
On INTEL Specification Change:
Change 1.00V (Nominal) Regulator to 1.05V (Nominal)
The 82567 has been updated to support both 1.8V and 1.9V

NOTE:

82567LM(AMT) is for Business
82567LF (non AMT) is for Consumer
82567V (non AMT) is for Consumer

PEGATRON DT-MB RESTRICTED SECRET

PEGATRON		Title : INTEL 82567LAN	
Pegatron Corp.		Engineer: Wesley_Tzeng	
Size A3	Project Name ZEUS-80		Rev 1.05
Date: Monday, October 12, 2009		Sheet 39 of 73	

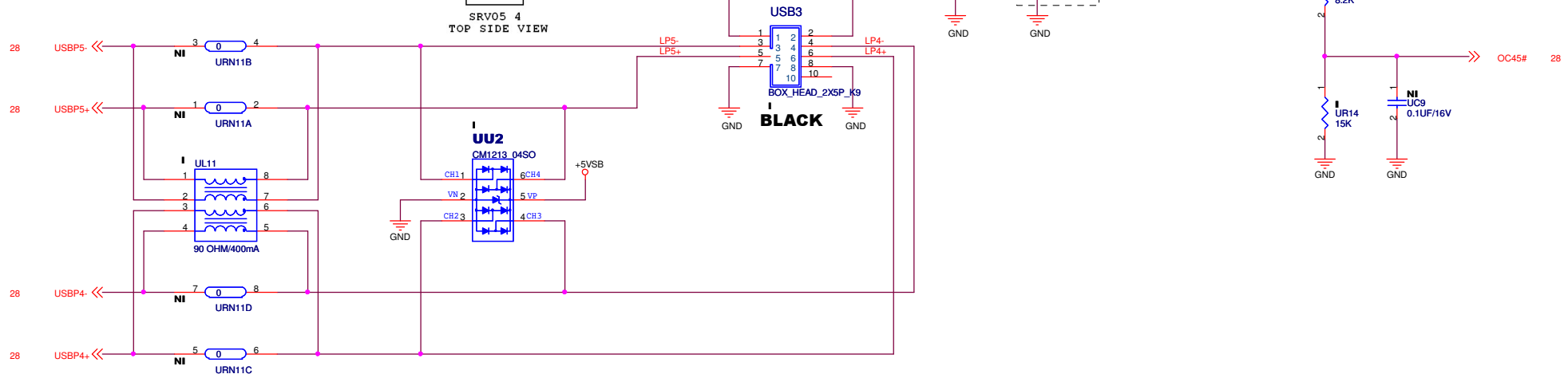
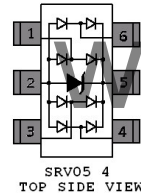
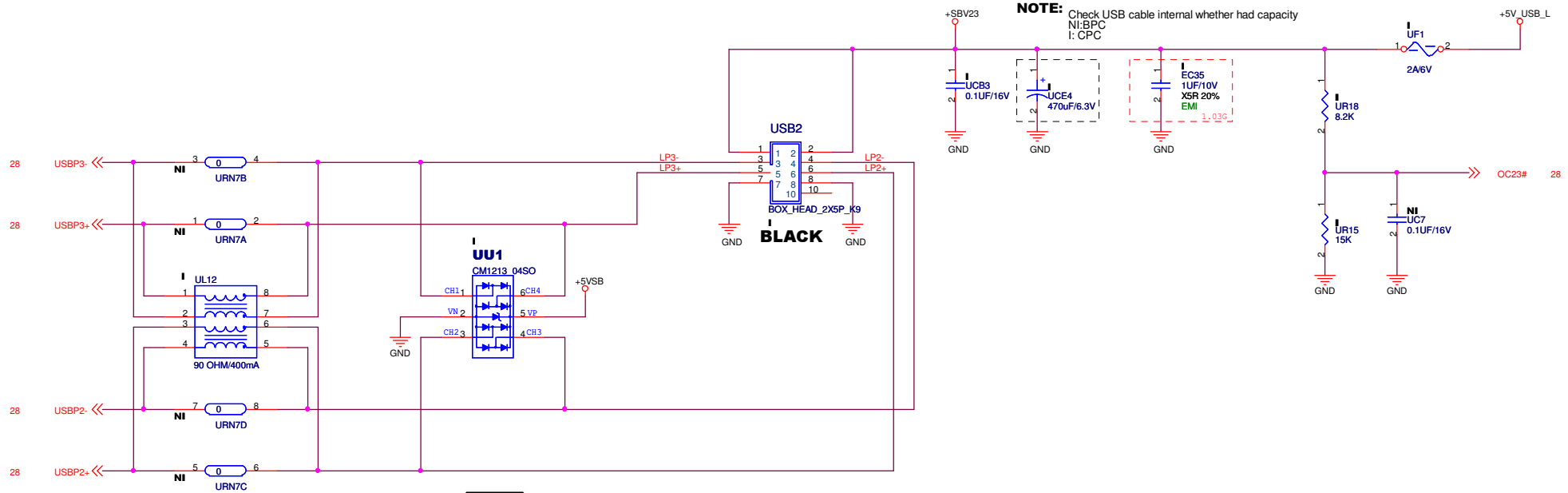


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PEGATRON DT-MB RESTRICTED SECRET

PEGATRON		Title : USB REAR CONNECTOR	
Pegatron Corp.		Engineer: Wesley_Tzeng	
Size A3	Project Name ZEUS-80	Rev 1.05	
Date: Monday, October 12, 2009		Sheet 41 of 74	

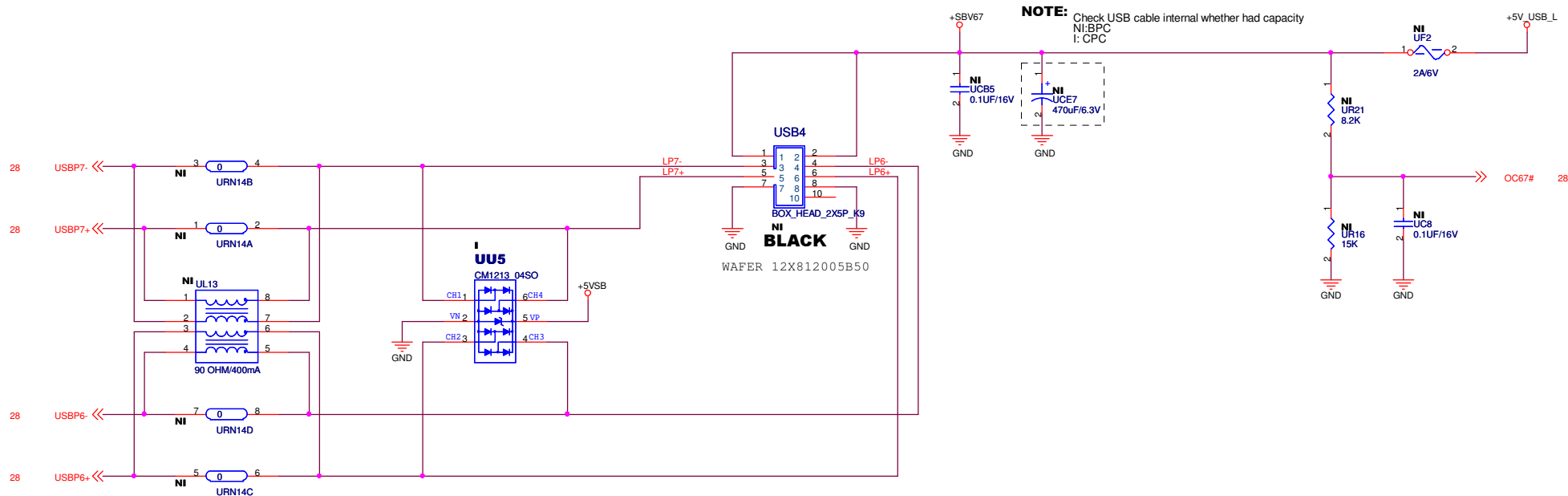
USB FRONT CONNECTOR - 1



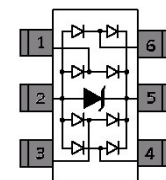
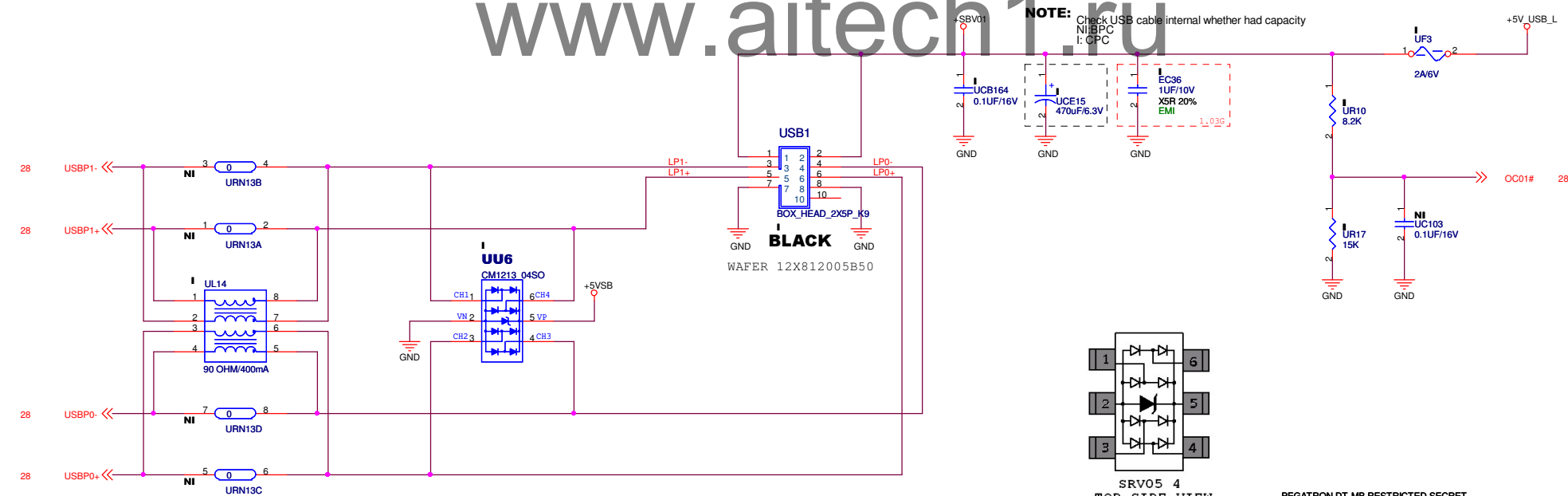
PEGATRON DT-MB RESTRICTED SECRET

PEGATRON		Title : USB FRONT CONNECTOR 1	
Pegatron Corp.		Engineer: Wesley_Tzeng	
Size A3	Project Name ZEUS-80	Rev 1.05	
Date: Monday, October 12, 2009		Sheet 42 of 74	

USB FRONT CONNECTOR - 2

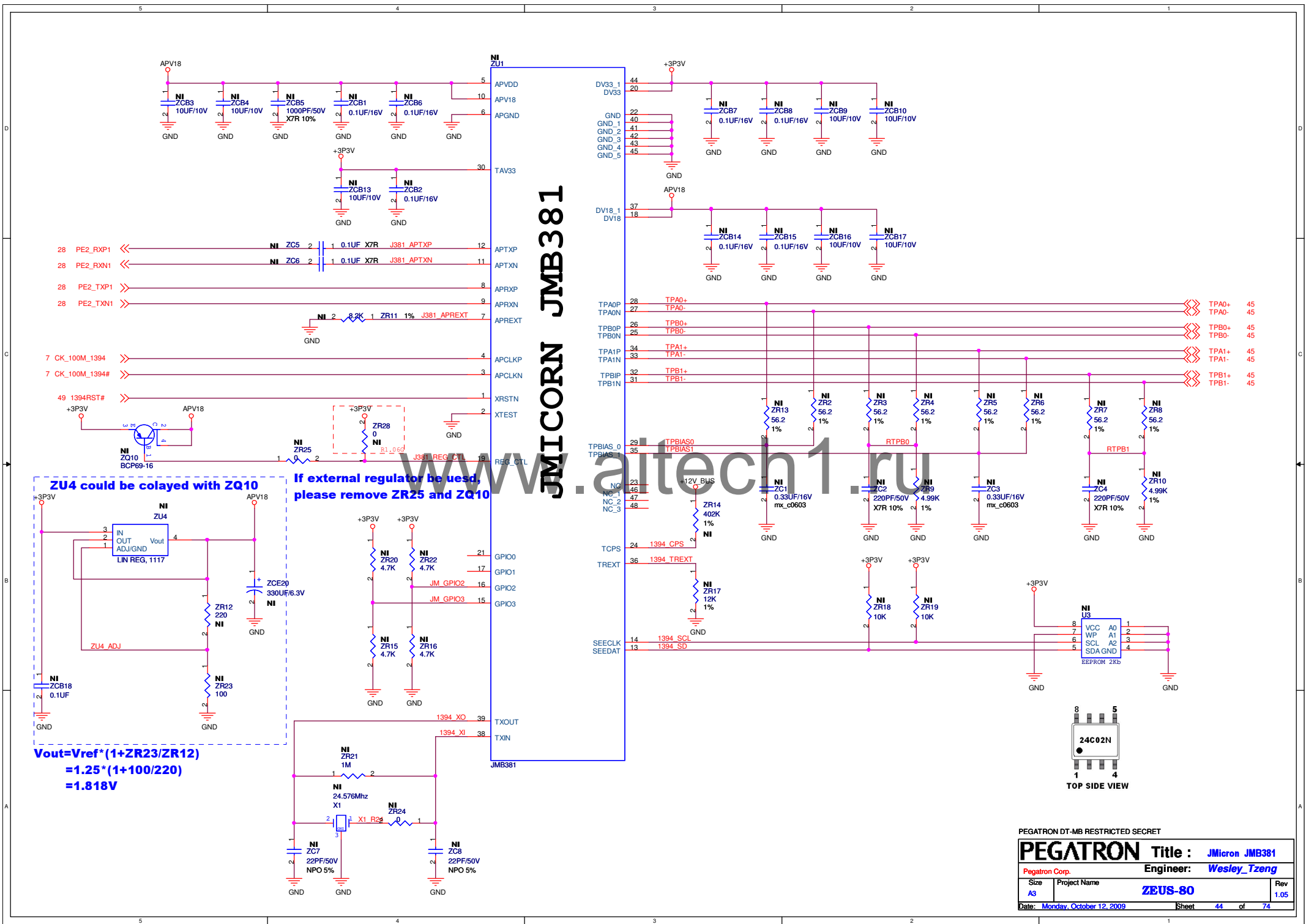


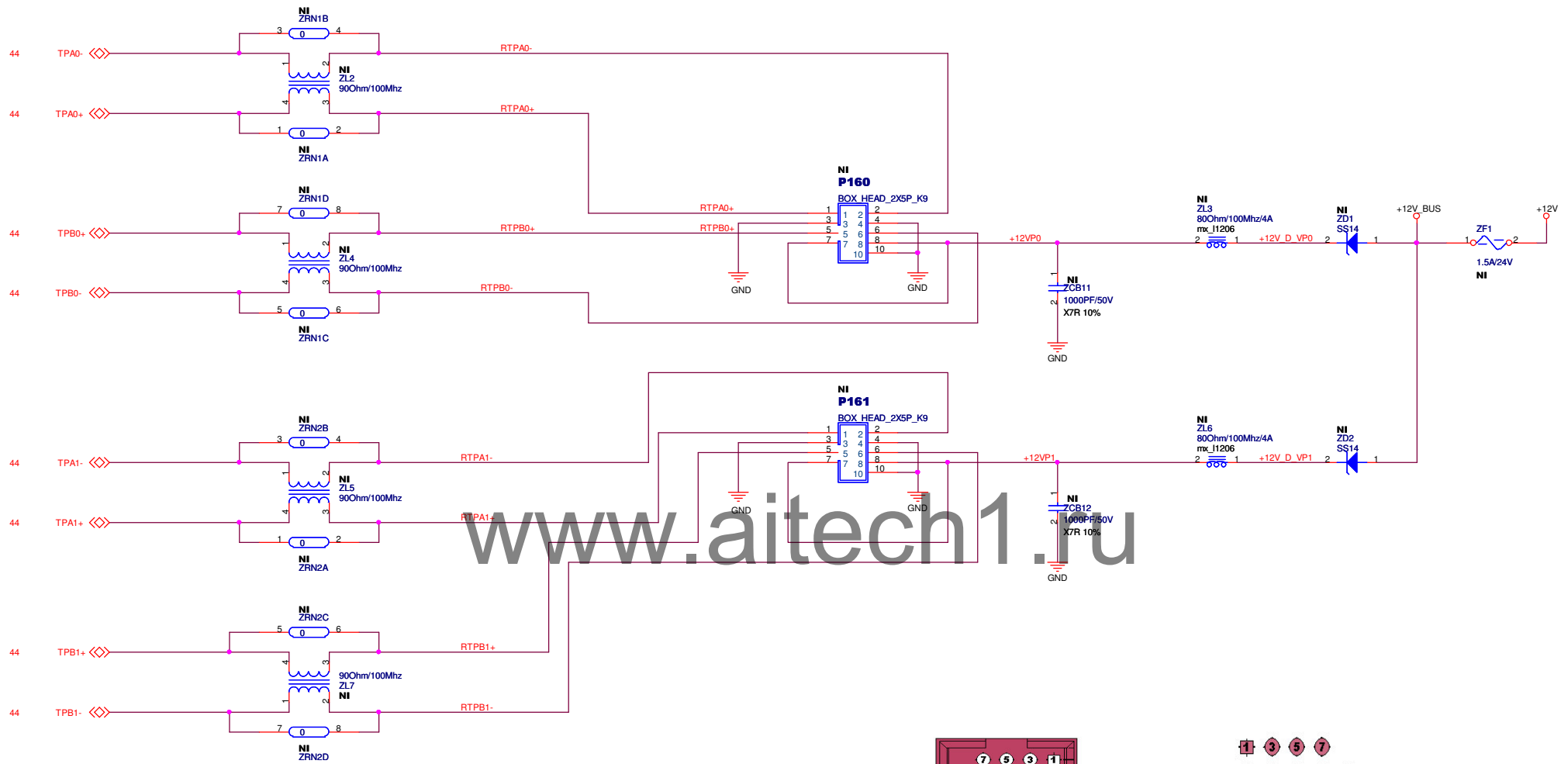
www.aitech1.ru



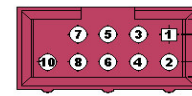
PEGATRON DT-MB RESTRICTED SECRET

PEGATRON		Title :USB FRONT CONNECTOR 2	
Pegatron Corp.		Engineer: Wesley_Tzeng	
Size A3	Project Name ZEUS-80	Rev 1.05	
Date: Monday, October 12, 2009		Sheet 43 of 74	

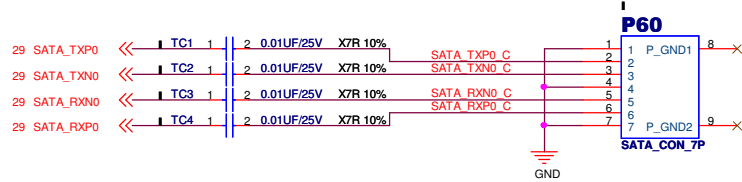




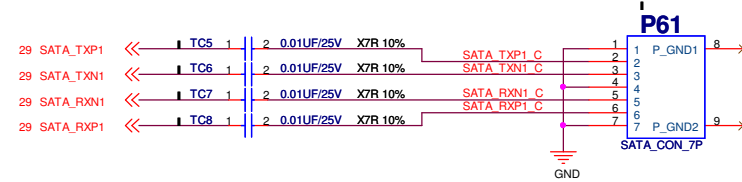
www.aitech1.ru



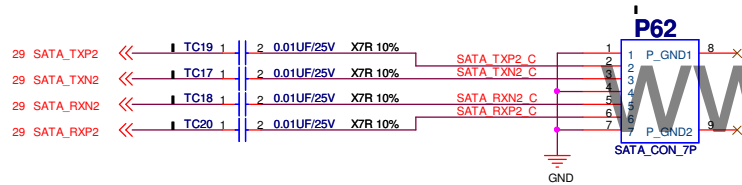
SATA CONNECTOR FOR BPC



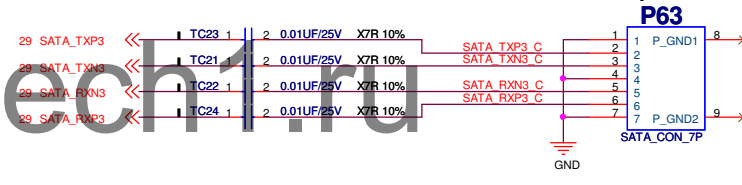
**SATA CONTROLLER #1
(PRIMARY MASTER)
COLOR = RED**



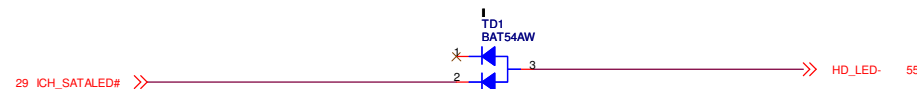
**SATA CONTROLLER #1
(SECONDARY MASTER)
COLOR = BLACK**



**SATA CONTROLLER #1
(SECONDARY MASTER)
COLOR = BLACK**



**SATA CONTROLLER #1
(SECONDARY MASTER)
COLOR = BLACK**



PEGATRON DT-MB RESTRICTED SECRET

PEGATRON		Title : SATA CONNECTORS	
Pegatron Corp.		Engineer: Wesley_Tzeng	
Size A3	Project Name ZEUS-80		Rev 1.05
Date: Monday, October 12, 2009		Sheet 46 of 74	



SOUT1=0 : 2E
SOUT1=1 : 4E(Default)

SOUT2=0 : SPI_ENABLE
SOUT2=1 : SPI_DISABLE(Default)

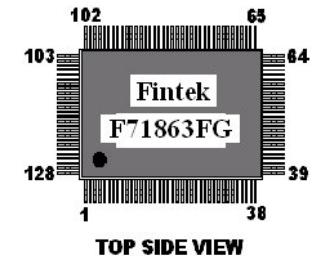
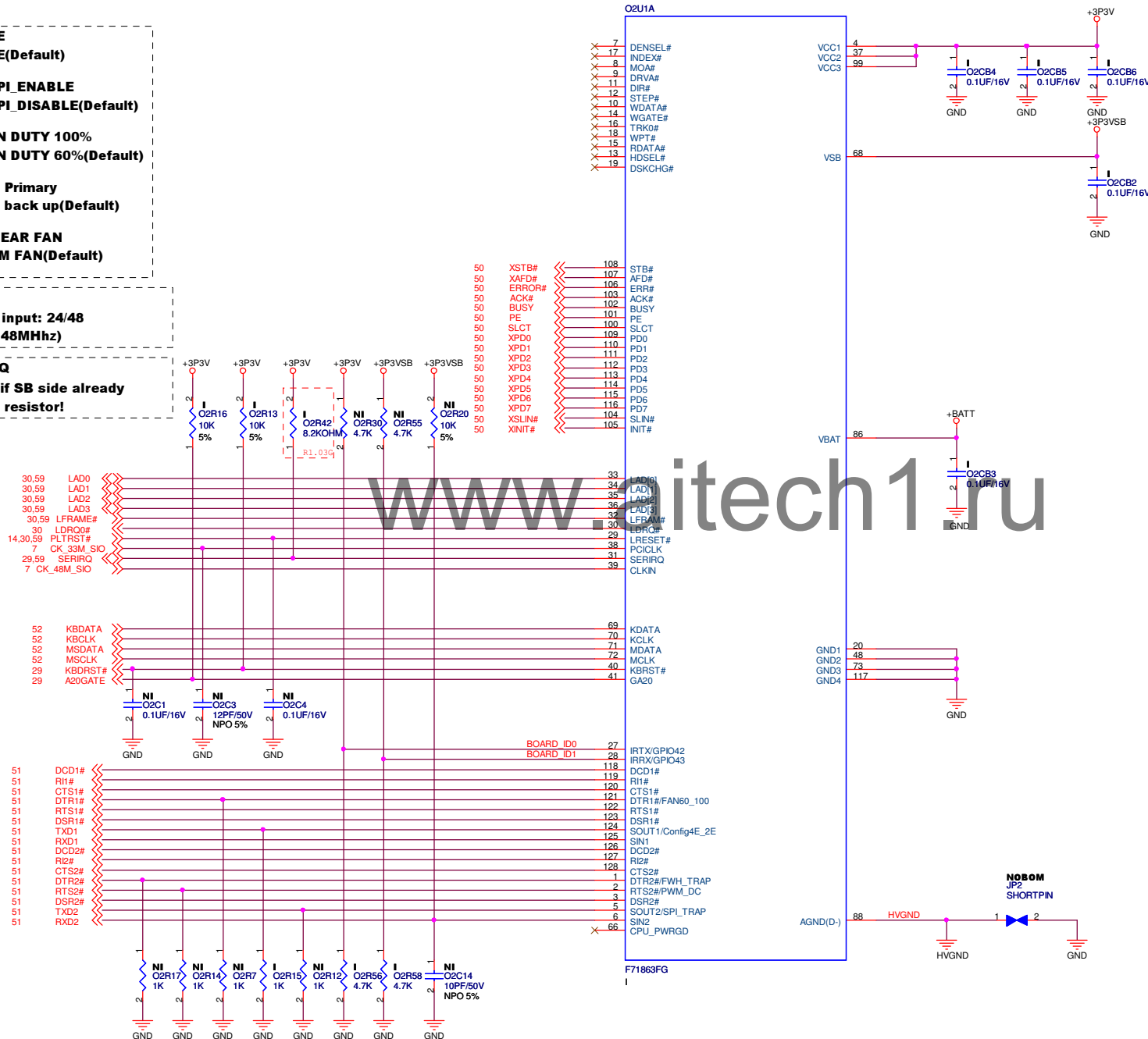
DTR1=0 : FAN DUTY 100%
DTR1=1 : FAN DUTY 60%(Default)

DTR2=0 : SPI Primary
DTR2=1 : SPI back up(Default)

RTS2=0 : LINEAR FAN
RTS2=1 : PWM FAN(Default)

Pin39:
System clock input: 24/48
MHz (Deault : 48MHz)

Pin 31: SERIRQ
Please check if SB side already
have a pull-up resistor!

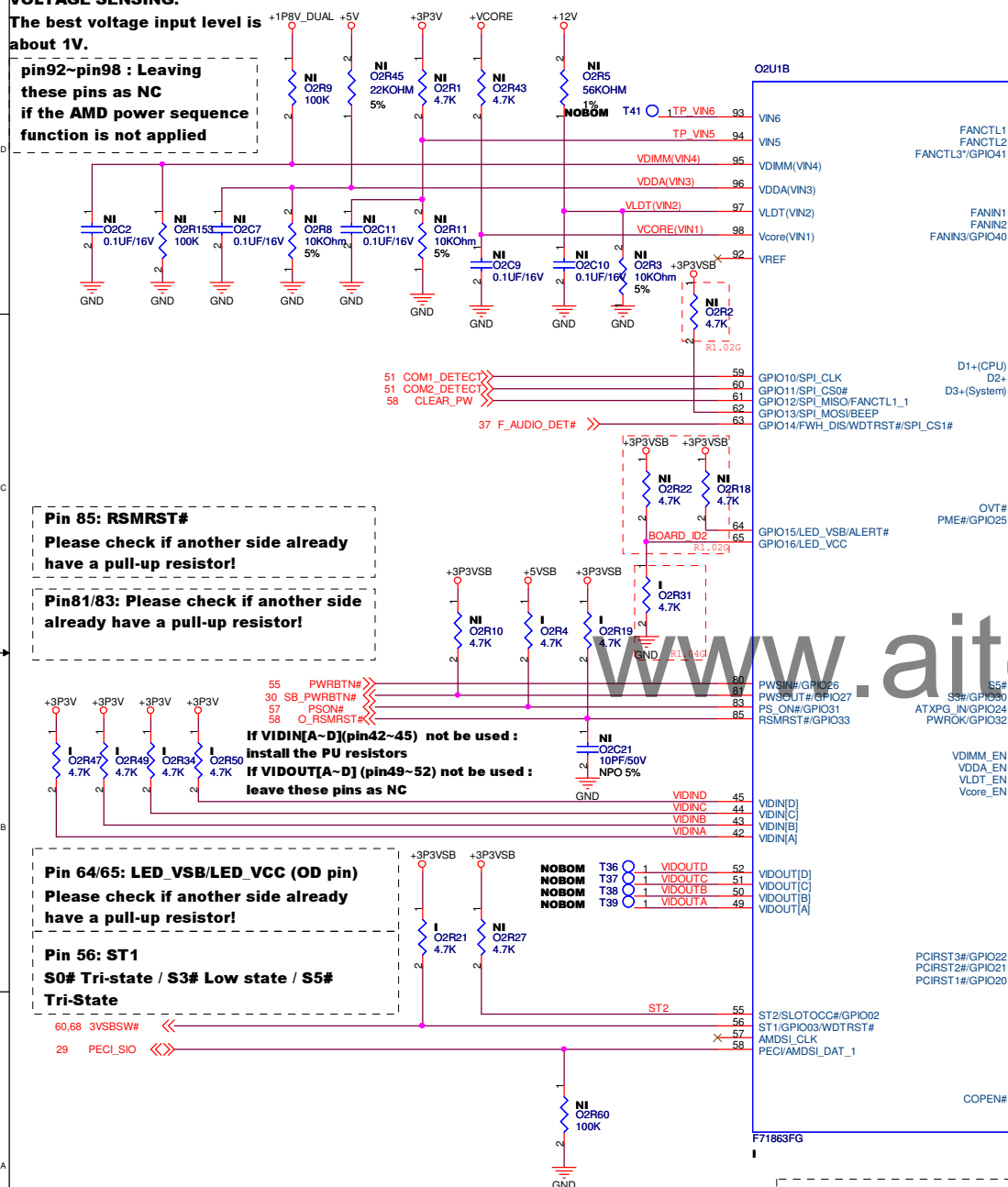


PEGATRON DT-MB RESTRICTED SECRET

PEGATRON		Title : SIO F71862 1 - 2	
Pegatron Corp.		Engineer: Wesley_Tzeng	
Size A3	Project Name ZEUS-80	Rev 1.05	
Date: Monday, October 12, 2009		Sheet 48	of 74

The best voltage input level is about 1V.

**pin92~pin98 : Leaving
these pins as NC
if the AMD power sequence
function is not applied**



Please check if another side already have a pull-up resistor!

Pin81/83: Please check if another side already have a pull-up resistor!

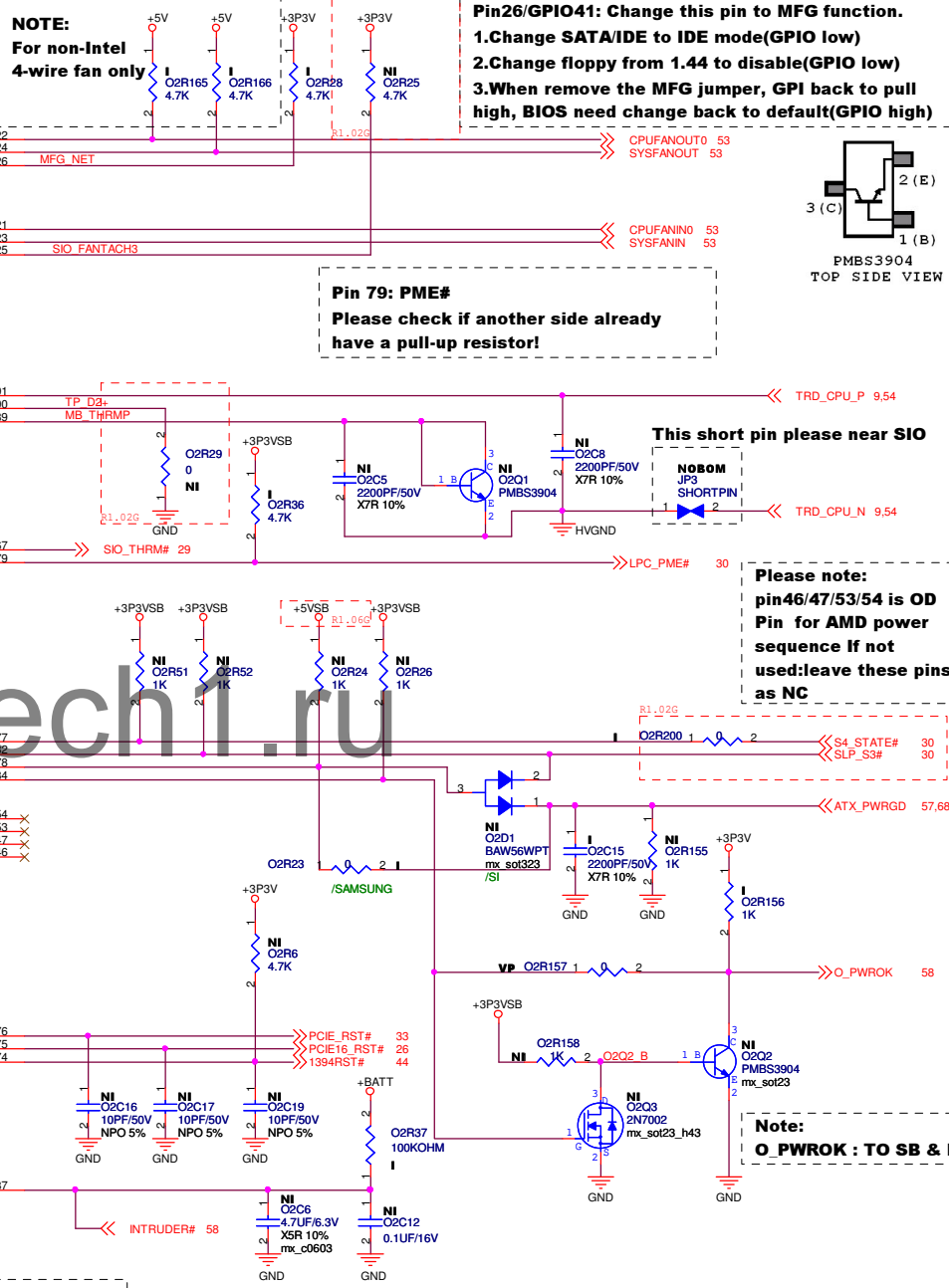
Pin 64/65: LED_VSB/LED_VCC (OD pin)
Please check if another side already
have a pull-up resistor!

Pin 56: ST1
S0# Tri-state / S3# Low state / S5#
Tri-State

Pin 55: ST2
Please add pull-up res if this pin as **SLOTCC#**!

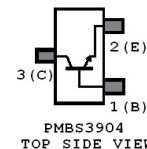
Pin 87: COPEN#
Please check if another side already have a pull-up resistor!

NOTE:
For non-Intel
4-wire fan only



Pin26/GPIO41: Change this pin to MFG function.

- 1.Change SATA/IDE to IDE mode(GPIO low)**
- 2.Change floppy from 1.44 to disable(GPIO low)**
- 3.When remove the MFG jumper, GPI back to pull high, BIOS need change back to default(GPIO high)**



Pin 79: PME#
Please check if another side already have a pull-up resistor!

This short pin please near SIO

Please note:
pin46/47/53/54 is OD
Pin for AMD power
sequence If not
used:leave these pins
as NC

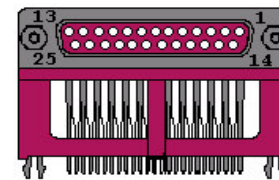
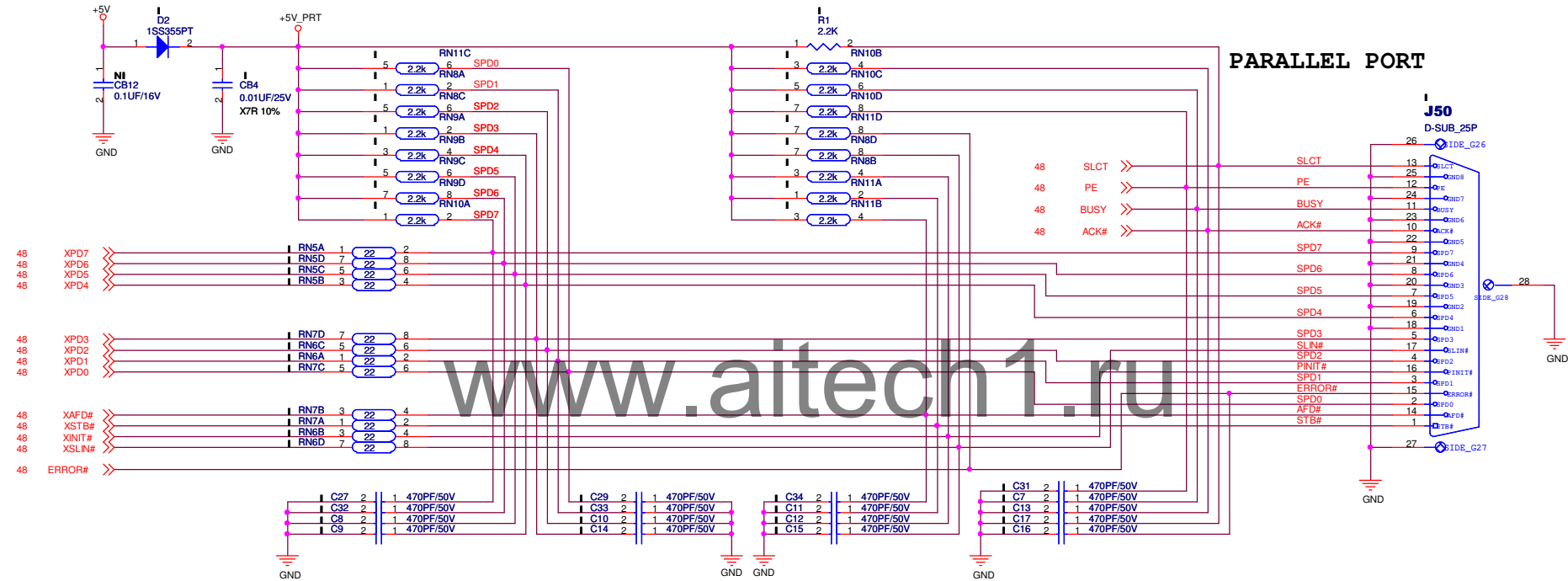
Note:
O PWROK : TO SB & NB

PEGATRON DT-MB RESTRICTED SECRET

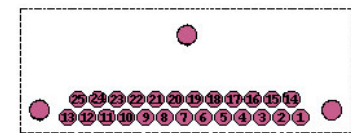
PEGATRON Title : SIO F71862 2 - 2

Pegatron Corp.		Engineer:	Wesley_Tzeng
Size A3	Project Name	ZEUS-80	Rev 1.05
Date:	Monday, October 12, 2009	Sheet	49 of 74

<< FOR CPC >>



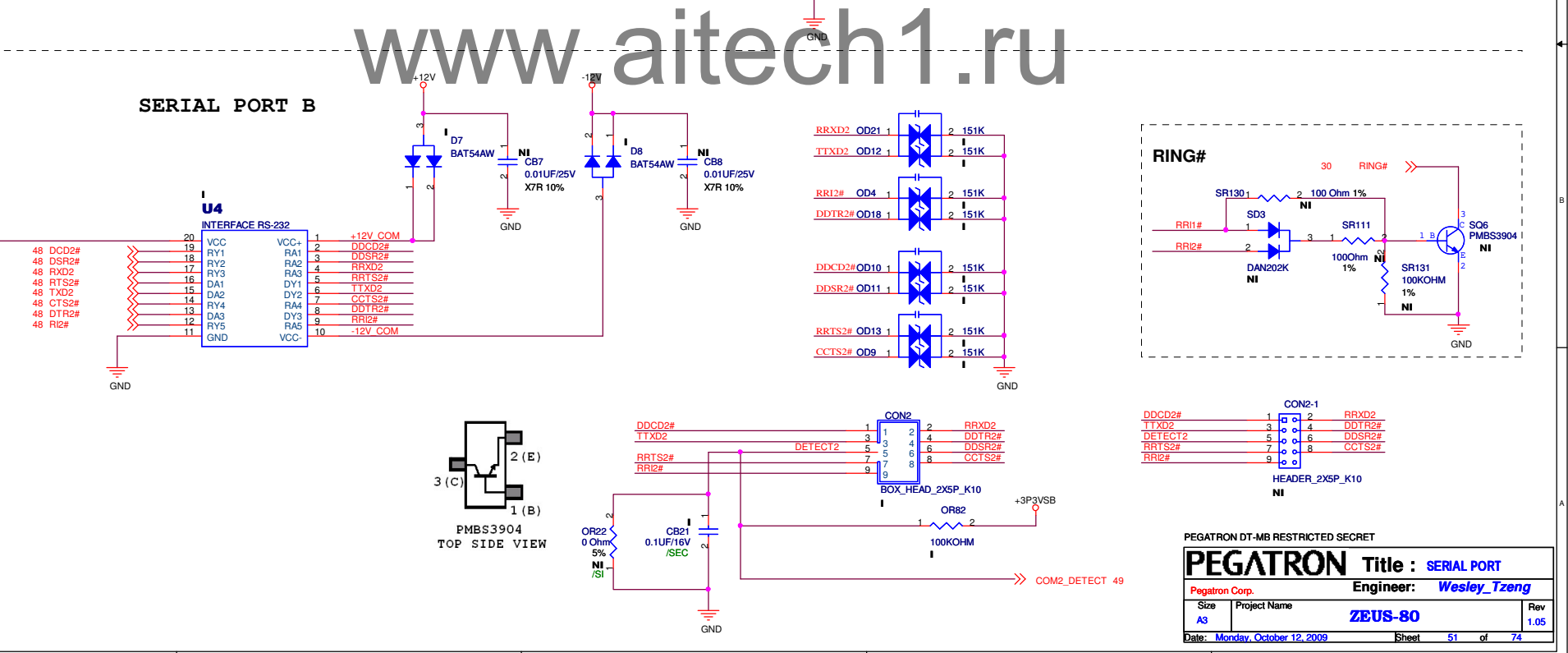
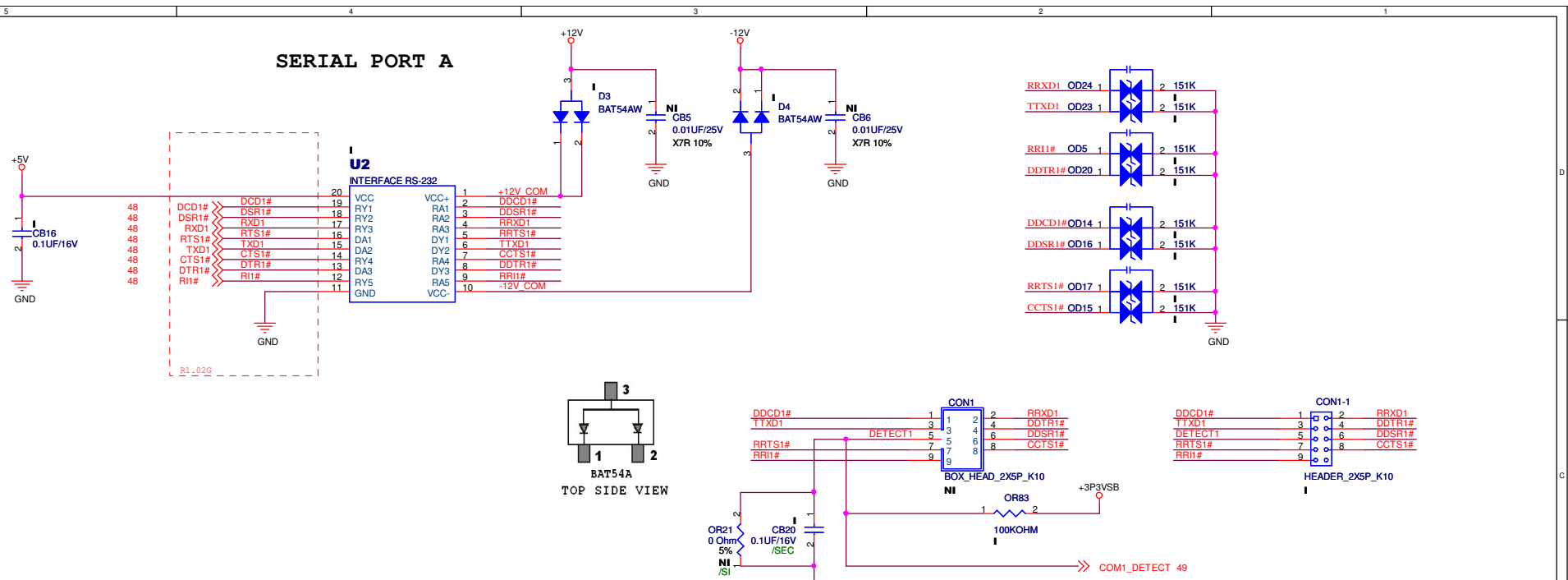
TOP SIDE VIEW



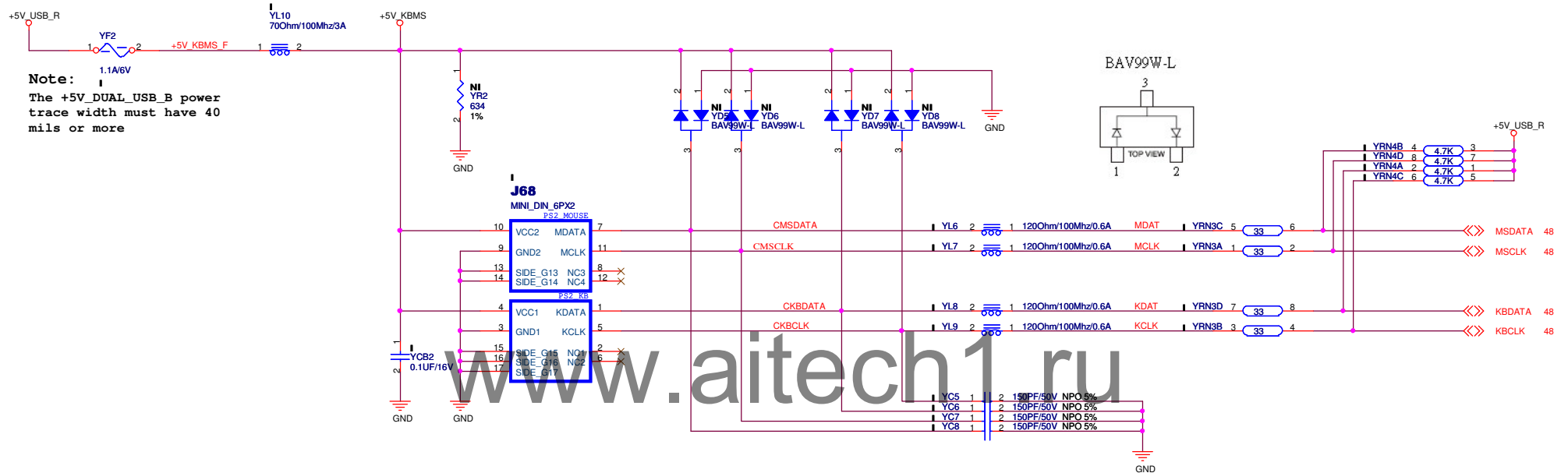
BOTTOM SIDE VIEW

PEGATRON DT-MB RESTRICTED SECRET

PEGATRON		Title : PARALLEL PORT - 2	
Pegatron Corp.		Engineer: Wesley_Tzeng	
Size	Project Name	ZEUS-80	
A3			Rev 1.05
Date: Monday, October 12, 2009		Sheet 50	of 74



PS/2 KEYBOARD & MOUSE FOR CPC



PEGATRON DT-MB RESTRICTED SECRET

PEGATRON		Title : KB & MS FOR CPC	
Pegatron Corp.		Engineer: Wesley_Tzeng	
Size A3	Project Name ZEUS-80	Rev 1.05	
Date: Monday, October 12, 2009		Sheet 52 of 74	

5	
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QUAGGIO FANTASMA (OGAN)



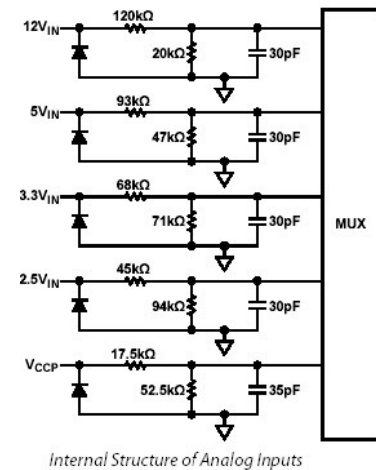
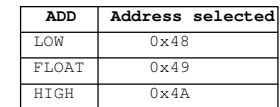
PEGATRON		Title : 4-PIN FAN CONN	
Pegatron Corp.		Engineer: Wesley_Tzeng	
Size A3	Project Name ZEUS-80	Rev 1.05	
Date: Monday, October 12, 2009		Sheet 53 of 74	

Pegatron Corp. Engineer: Wesley_Tzeng

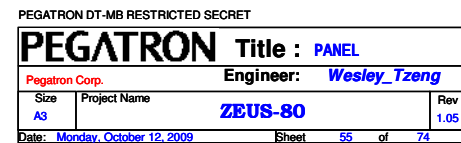
Size	Project Name	Rev
------	--------------	-----

A3	ZEUS-80			1.05
Date: Monday, October 12, 2009		Sheet	53	of 74

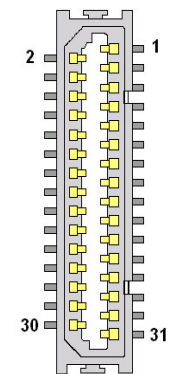
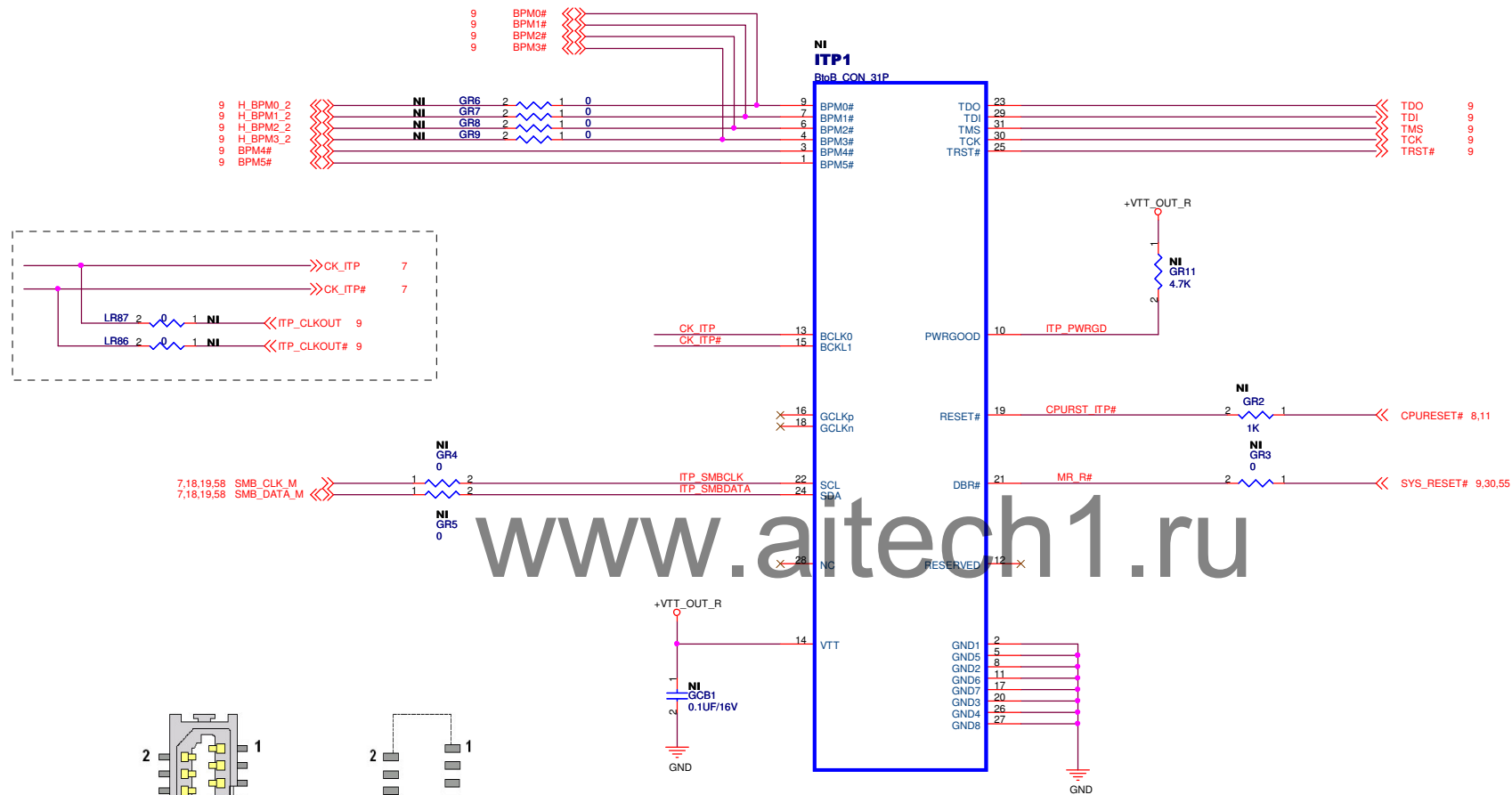
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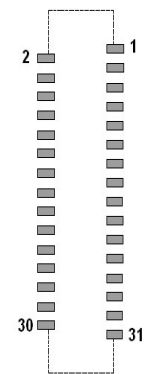
PEGATRON		Title : <i>H/W Monitor</i>	
<i>Pegatron Corp.</i>		Engineer: <i>Wesley_Tzeng</i>	
Size A3	Project Name ZEUS-80	Rev 1.05	
Date: Monday, October 12, 2009		Sheet	54 of 74



INTEL LGA-775 PROCESSOR ITP DEBUG PORT



HRS/DF9C-31S-1V(22)
TOP SIDE VIEW



HRS/DF9C-31S-1V(22)
PCB FOOTPRINT

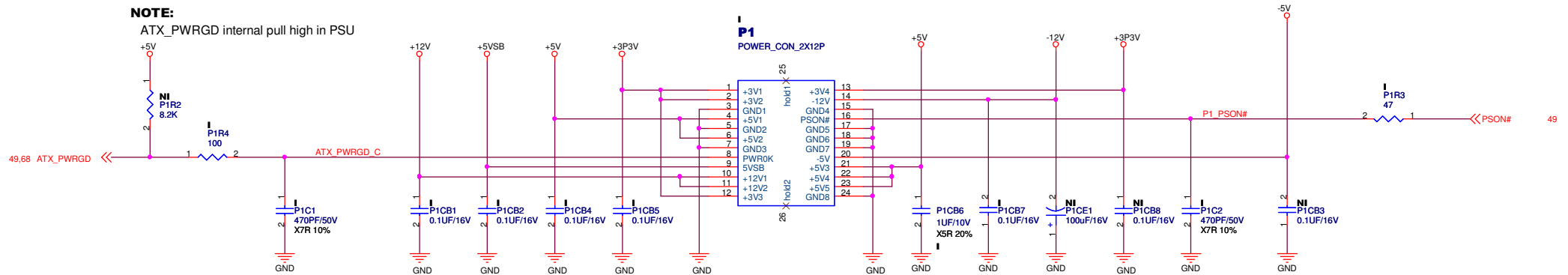
PEGATRON DT-MB RESTRICTED SECRET

PEGATRON		Title : ITP_31P CONN.	
Pegatron Corp.		Engineer: Wesley_Tzeng	
Size A3	Project Name ZEUS-80	Rev 1.05	
Date: Monday, October 12, 2009		Sheet 56 of 74	

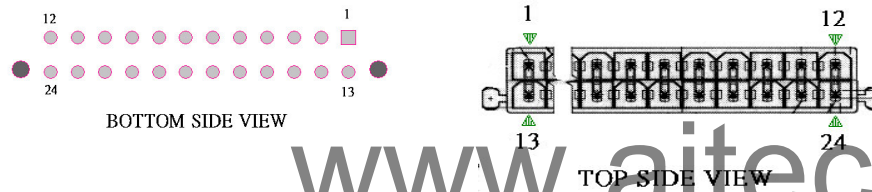
ATX POWER_24P SUPPLY CONNECTOR

NOTE:

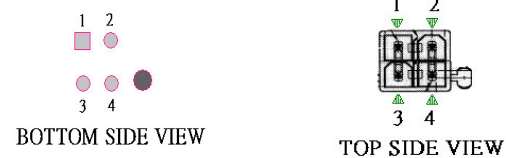
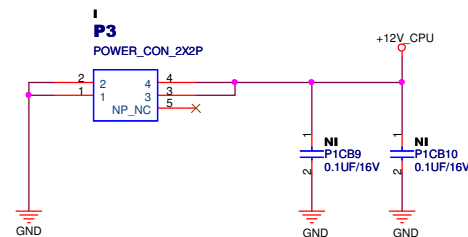
ATX_PWRGD internal pull high in PSU



All of the Caps Around the ATX Power Connector



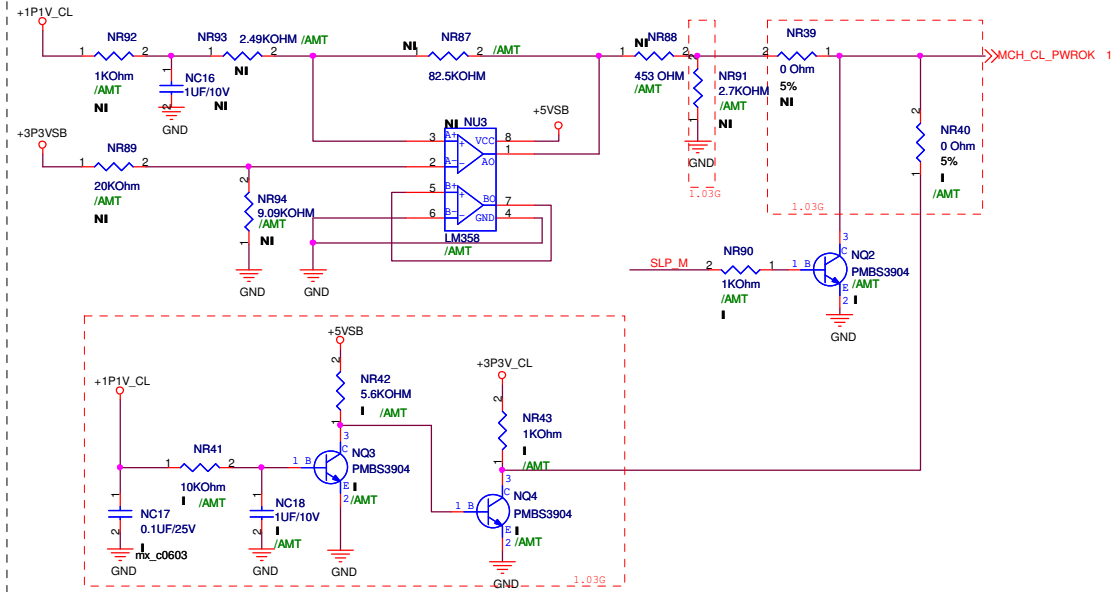
VRM POWER_4P SUPPLY CONNECTOR



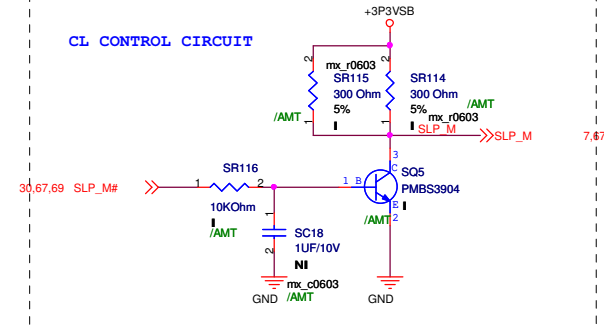
PEGATRON DT-MB RESTRICTED SECRET

PEGATRON		Title : ATX POWER	
Pegatron Corp.		Engineer: Wesley_Tzeng	
Size A3	Project Name ZEUS-80	Rev 1.05	
Date: Monday, October 12, 2009		Sheet 57	of 74

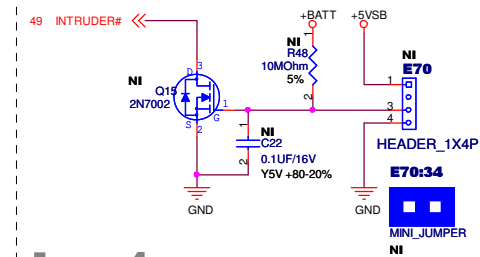
CLINK PWROK GENERATION



CL CONTROL CIRCUIT

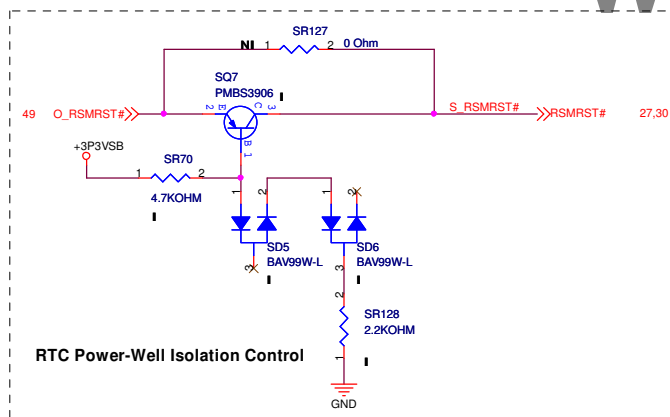


INTRUDER

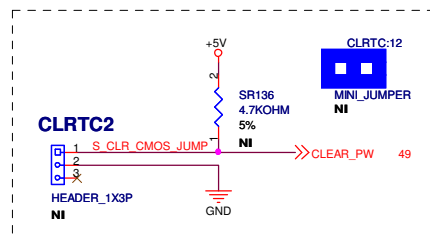


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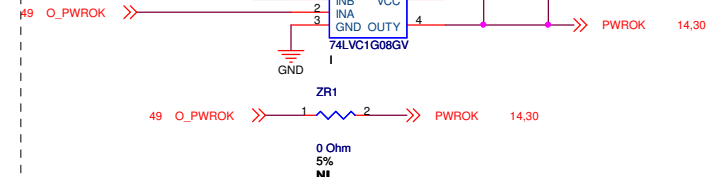
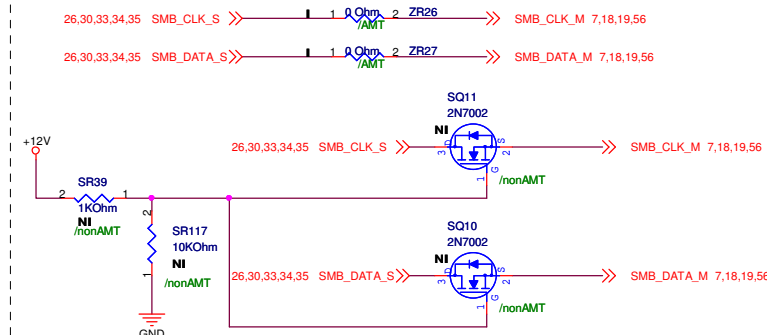
RTC Power-Well Isolation Control



CLRTC2



SMBus Switch



PEGATRON DT-MB RESTRICTED SECRET

PEGATRON		Title : CLINK PWROK	
Pegatron Corp.		Engineer: Wesley_Tzeng	
Size A3	Project Name ZEUS-80	Rev 1.05	
Date: Monday, October 12, 2009	Sheet 58	of 74	

TPM

TOP SIDE VIEW

30,48 LAD3 <<<

30,48 LAD2 <<<

30,48 LAD1 <<<

30,48 LAD0 <<<

30,48 LFRAME# <<<

29,48 SERIRQ <<<

7 CK_33M_TPM >>>

14,30,48 PLTRST# >>>

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TPM_BASE_ADDR	I/O SPACE
0	2E
1	4E

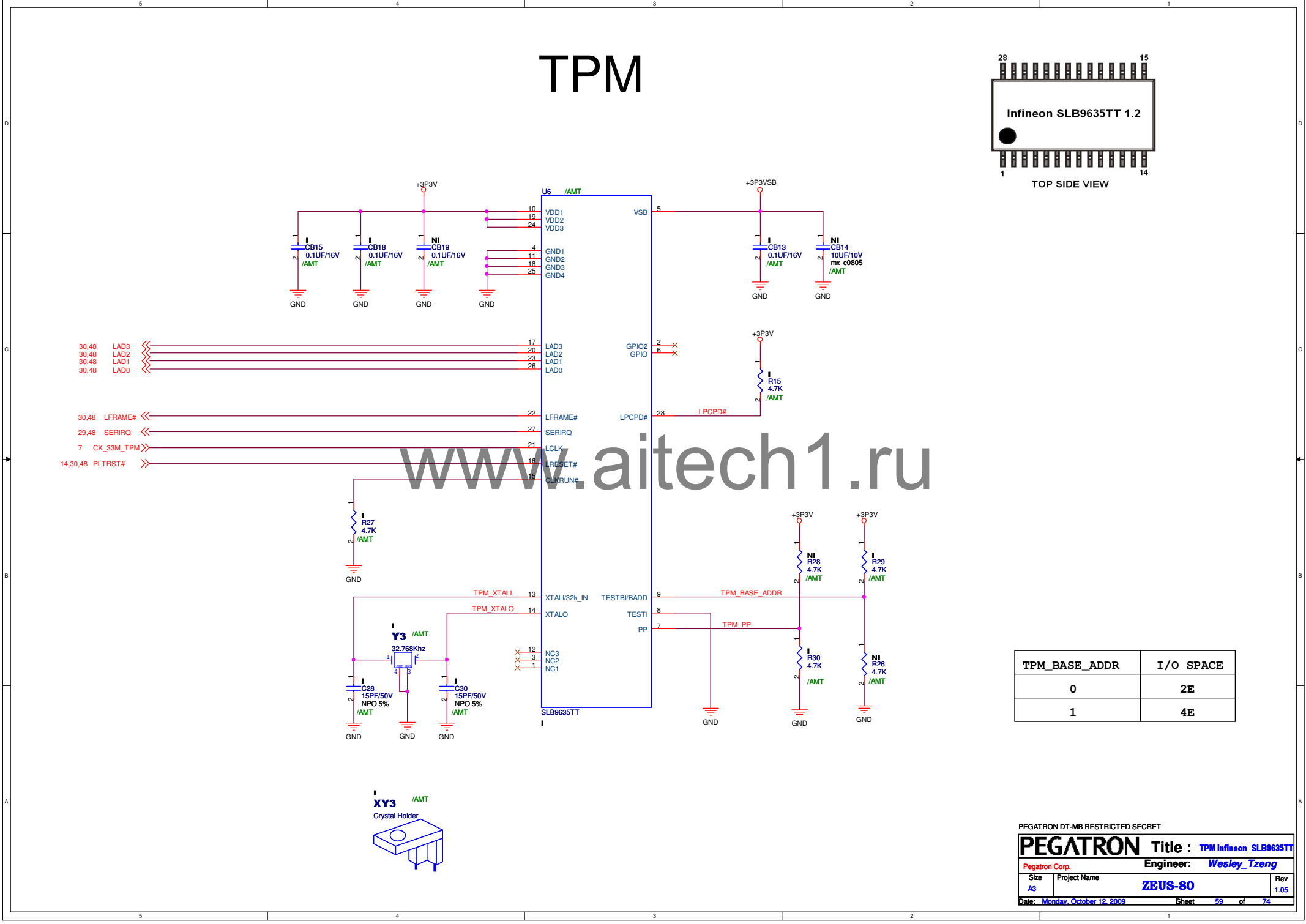
PEGATRON DT-MB RESTRICTED SECRET

PEGATRON Title : TPM infineon_SLB9635TT

Engineer: Wesley_Tzeng

Size A3 Project Name ZEUS-80 Rev 1.05

Date: Monday, October 12, 2009 Sheet 59 of 74

[illegible]

TPM

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TOP SIDE VIEW

TPM_BASE_ADDR	I/O SPACE
0	2E
1	4E

XY3
Crystal Holder

PEGATRON DT-MB RESTRICTED SECRET

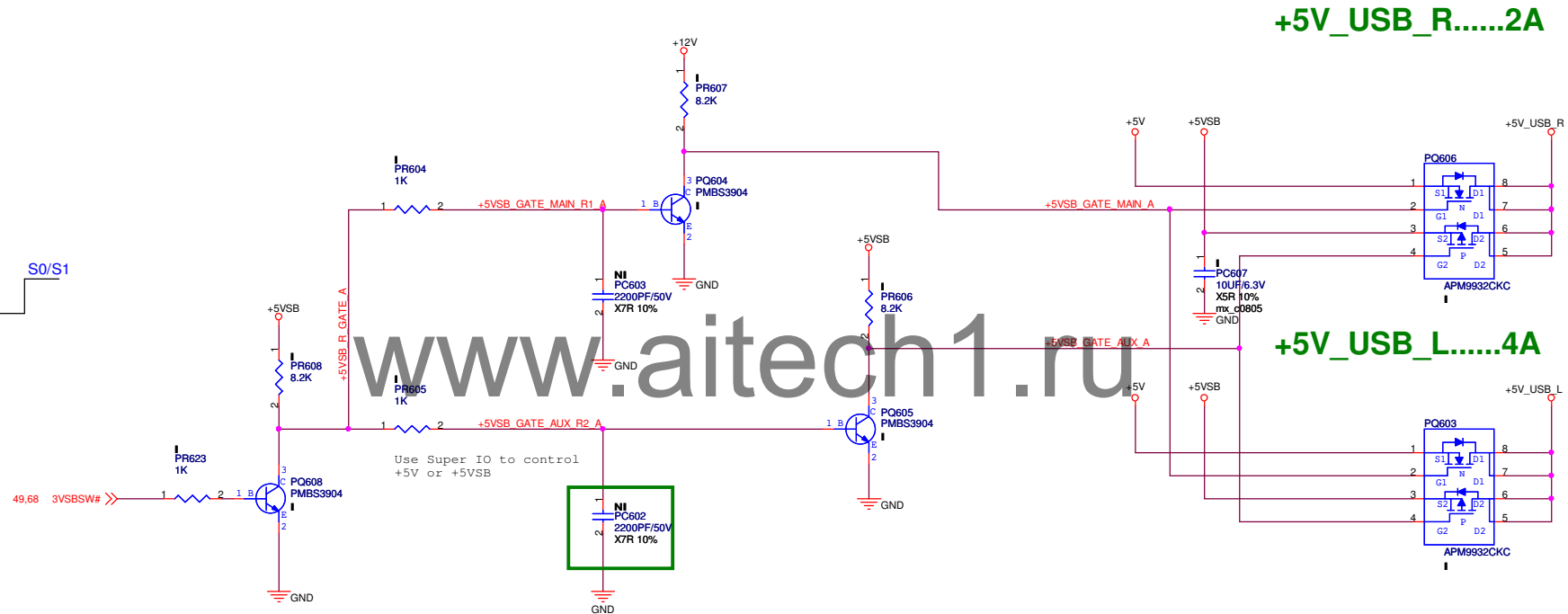
PEGATRON Title : TPM infineon_SLB9635TT

Engineer: Wesley_Tzeng

Size A3 Project Name ZEUS-80 Rev 1.05

Date: Monday, October 12, 2009 Sheet 59 of 74

[illegible][illegible]



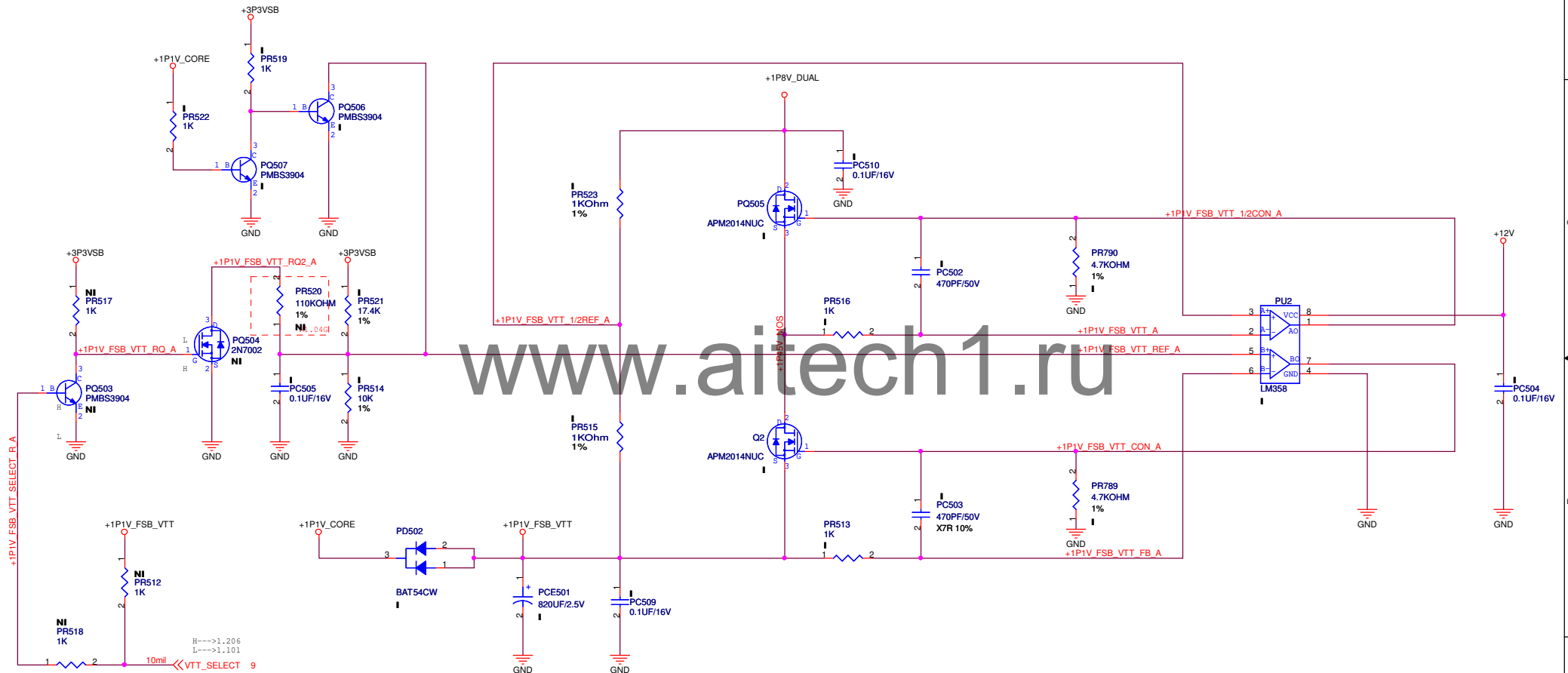
PEGATRON DT-MB RESTRICTED SECRET

PEGATRON		Title : +5V_DUAL & +5V_DUAL_USB_F	
Pegatron Corp.		Engineer: Wesley_Tzeng	
Size	Project Name	ZEUS-80	
A3		Rev 1.05	
Date: Monday, October 12, 2009		Sheet	60 of 74

+1P1(1P2)V_FSB_VTT.....(1.1V) (NI)

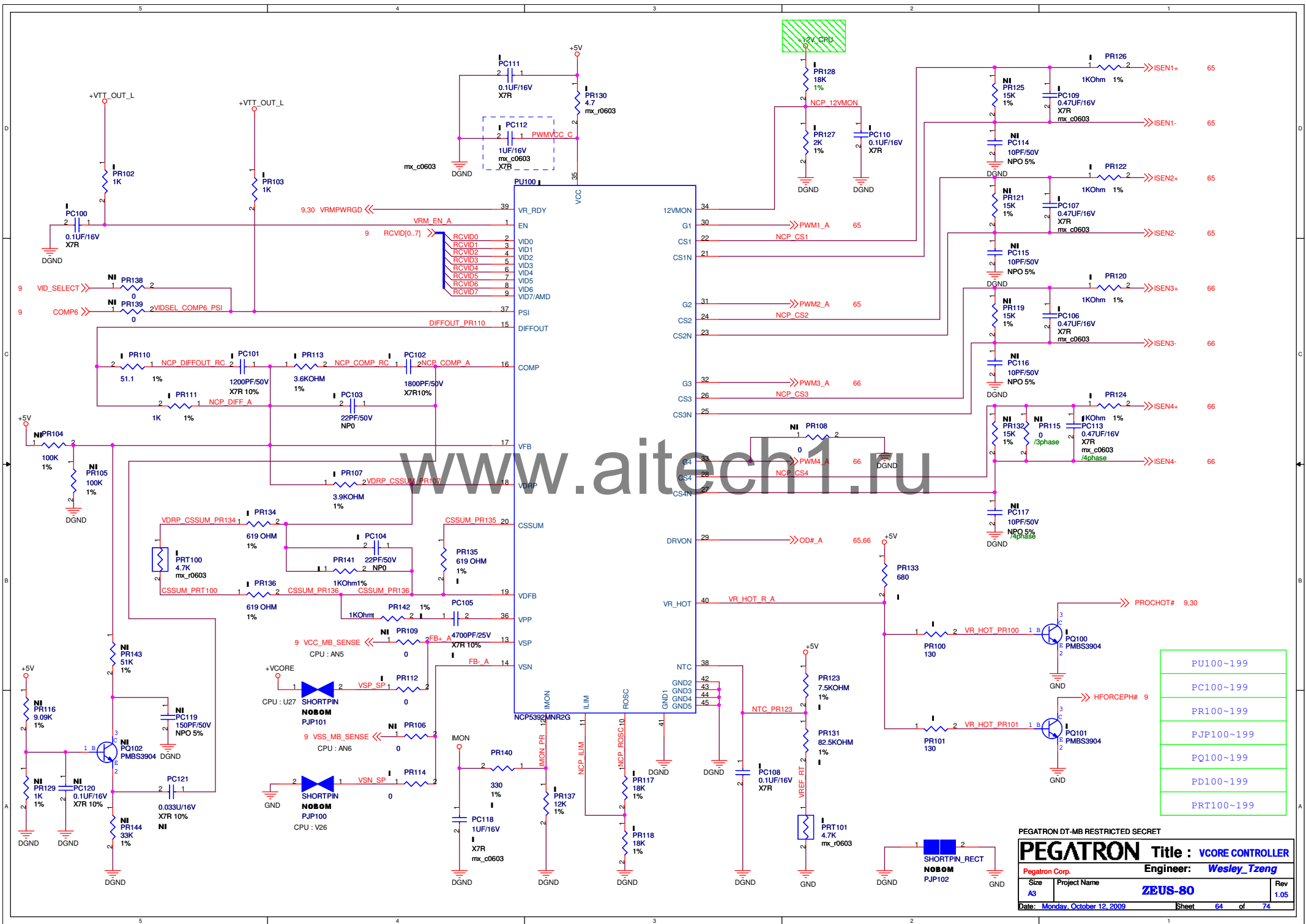
I_{max}=5.8A

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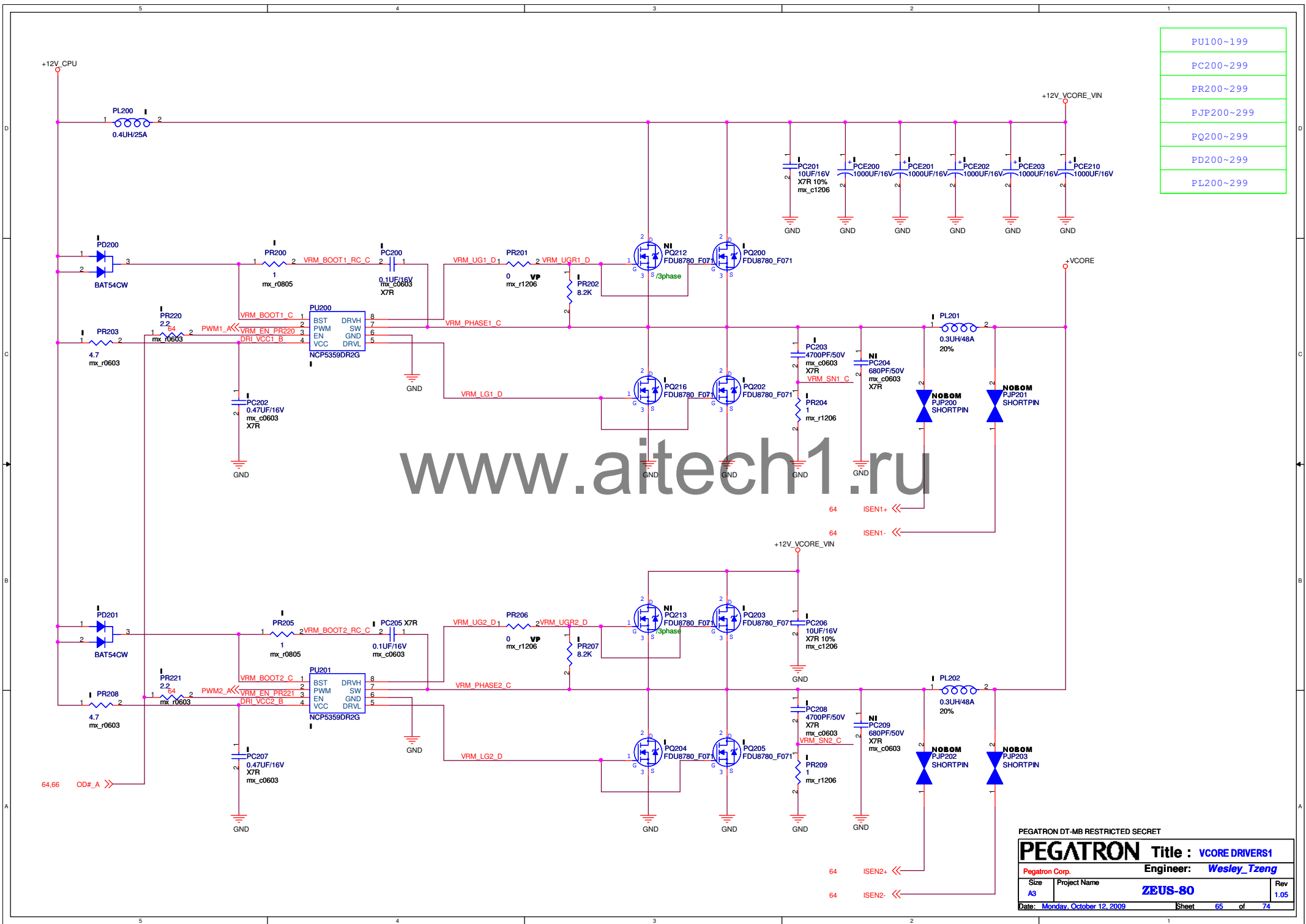
PEGATRON DT-MB RESTRICTED SECRET

PEGATRON		Title : +1P1V_FSB_VTT&1P5V_ICH	
Pegatron Corp.		Engineer: Wesley_Tzeng	
Size A3	Project Name ZEUS-80	Rev 1.05	
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- PU100~199
- PC100~199
- PR100~199
- PJP100~199
- PQ100~199
- PD100~199
- PRT100~199



PU100~199
PC200~299
PR200~299
PJP200~299
PQ200~299
PD200~299
PL200~299

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PEGATRON

Title : **VCORE DRIVERS1**

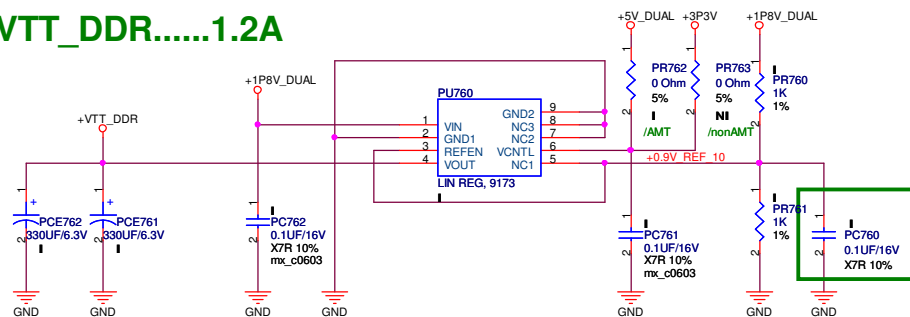
Pegatron Corp.

Engineer: **Wesley_Tzeng**

Size	Project Name	Rev
A3	ZEUS-80	1.05

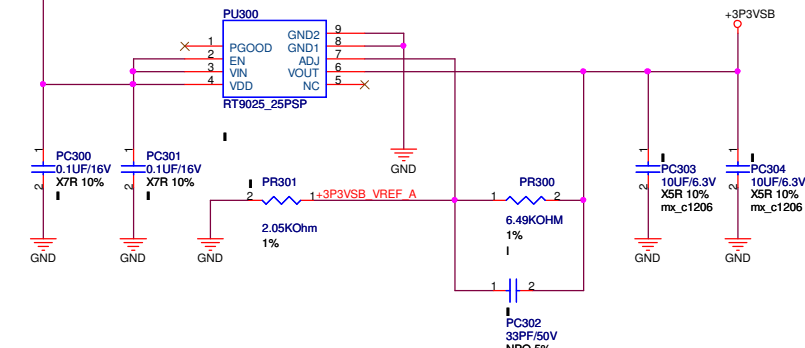
Date: Monday, October 12, 2009Sheet 65 of 74

+VTT_DDR.....1.2A

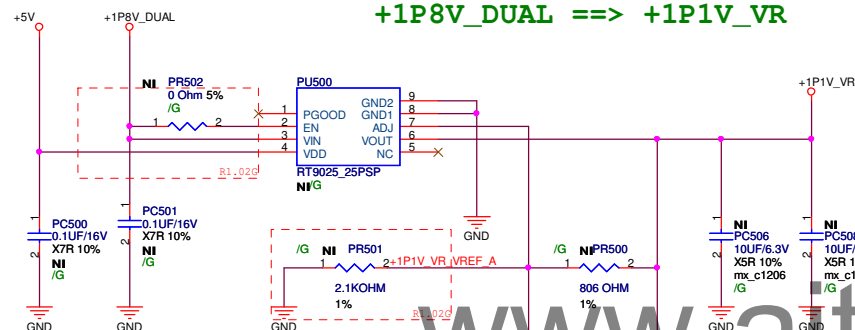


**CAE NOTE: PROVIDE 1.2cm x 1.2cm COPPER PAD
FOR DPAK(TO252) LET Tja OF 20C/W FOR 1.2A ON DDR VTT**

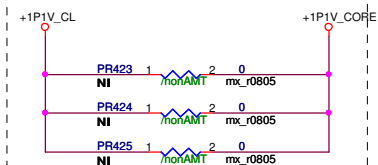
**+3P3VSB.....(3.3V)
Imax=1.3A**



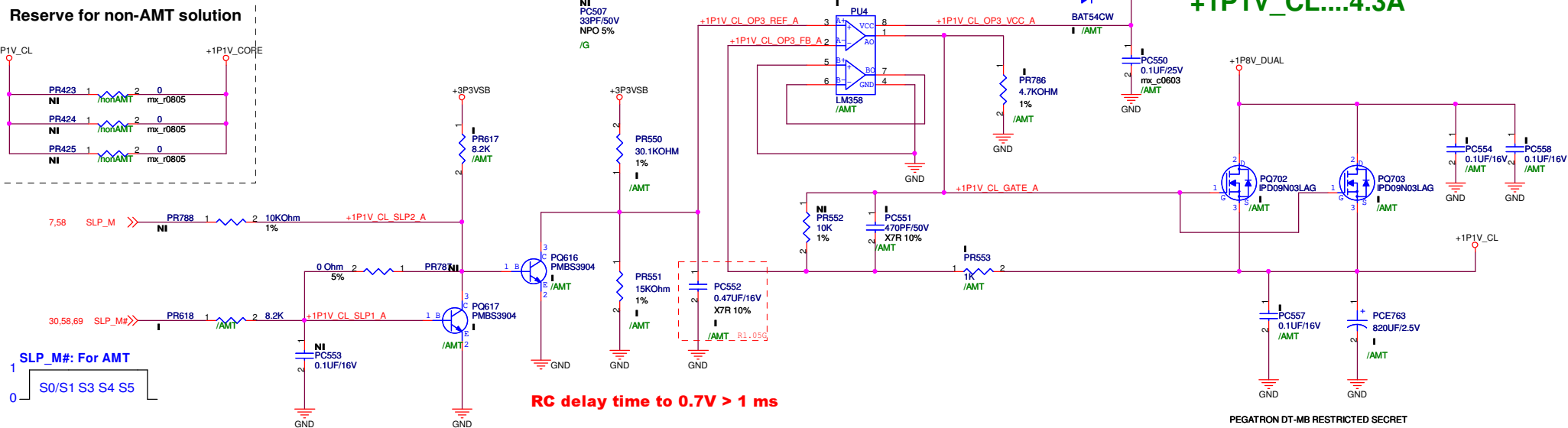
+1P8V_DUAL ==> +1P1V_VR



Reserve for non-AMT solution



+1P1V_CL....4.3A

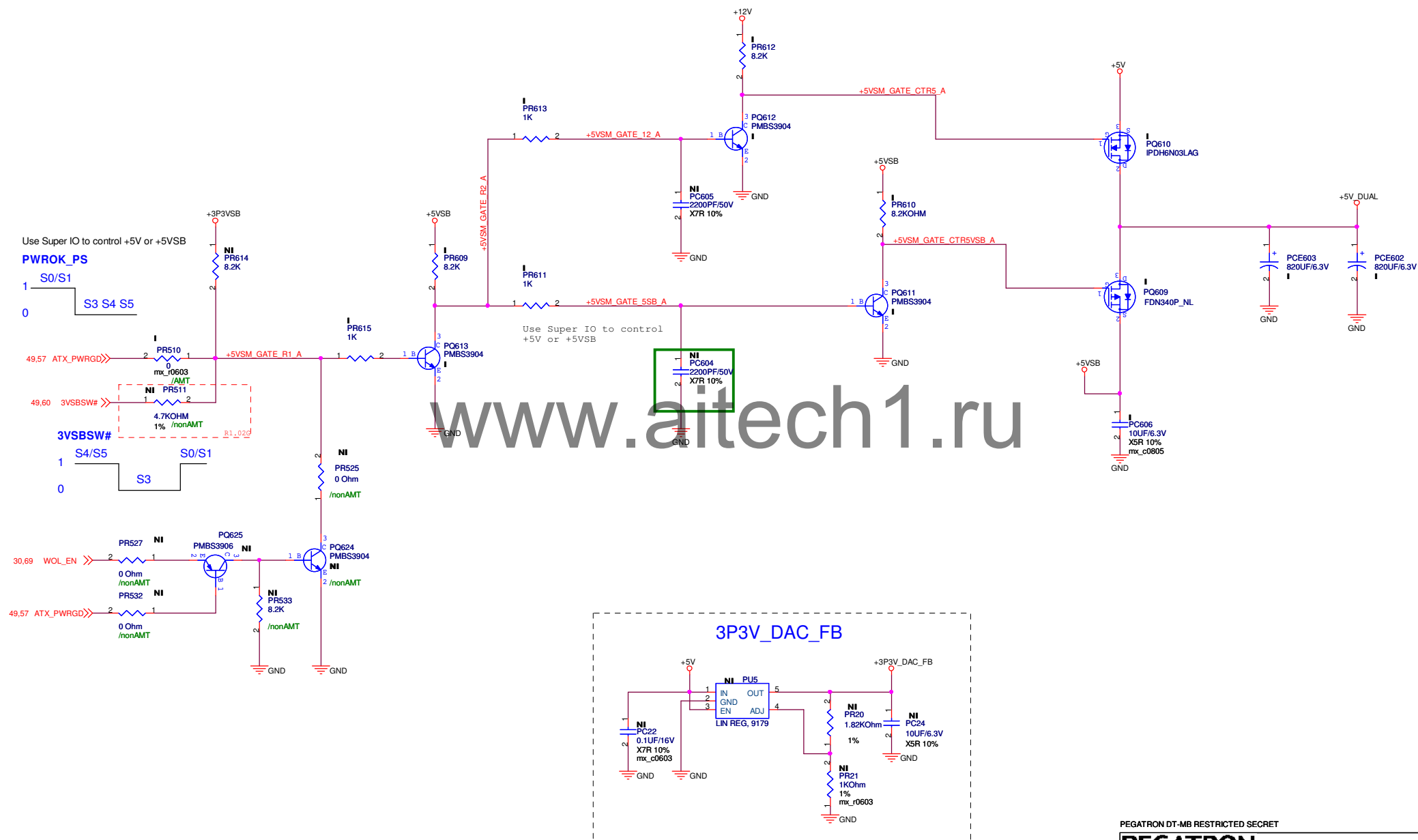


RC delay time to 0.7V > 1 ms

PEGATRON DT-MB RESTRICTED SECRET

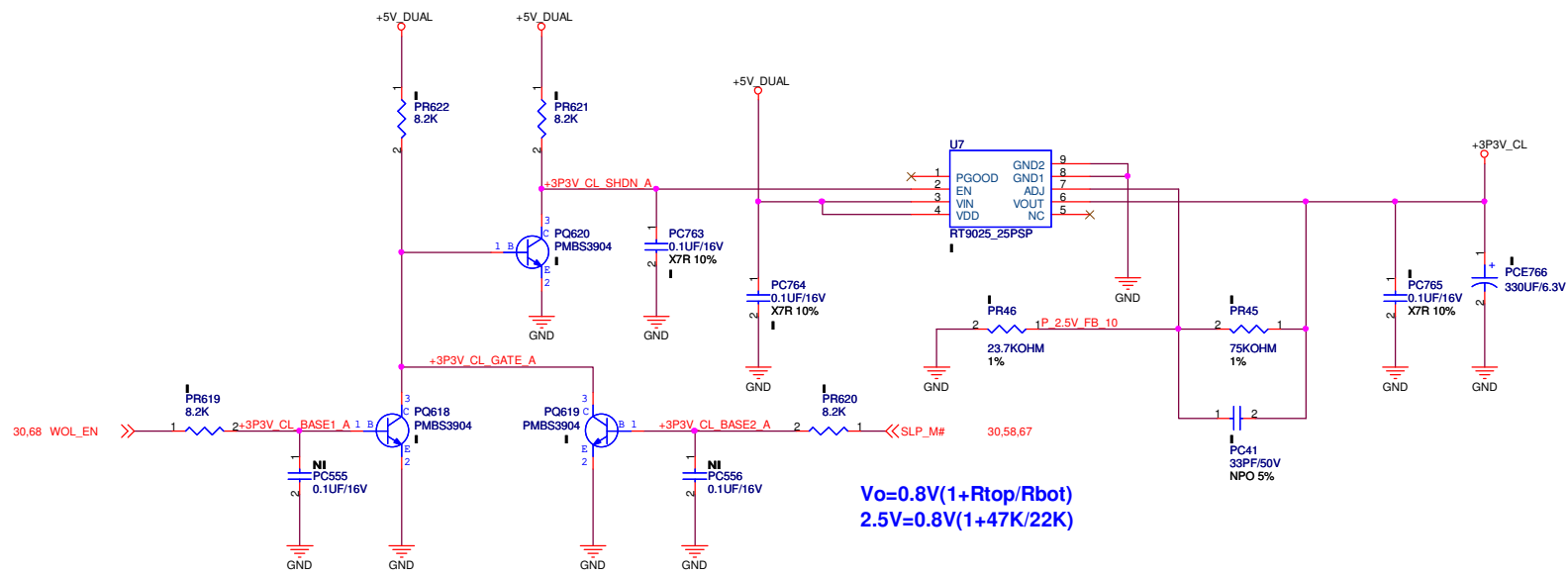
PEGATRON		Title : +3P3VSB & VTT_DDR & +1P5VSB	
Pegatron Corp.		Engineer: <i>Wesley_Tzeng</i>	
Size A3	Project Name ZEUS-80		Rev 1.05
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+5V_DUAL.....A



PEGATRON DT-MB RESTRICTED SECRET

PEGATRON		Title : +5V_DUAL	
Pegatron Corp.		Engineer: Wesley_Tzeng	
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+3P3V_CL

I_{max}=0.8A

+5V_DUAL => P_+3.3V_CL for WOL function(LAN:0.7A+others:0.1A)

WOL_EN & SLP_M#:

For AMT

1 S0/S1 S3 S4 S5
0

WOL_EN & SLP_M#:

For non-AMT

1 S0/S1 S0/S1
0 S3 S4 S5

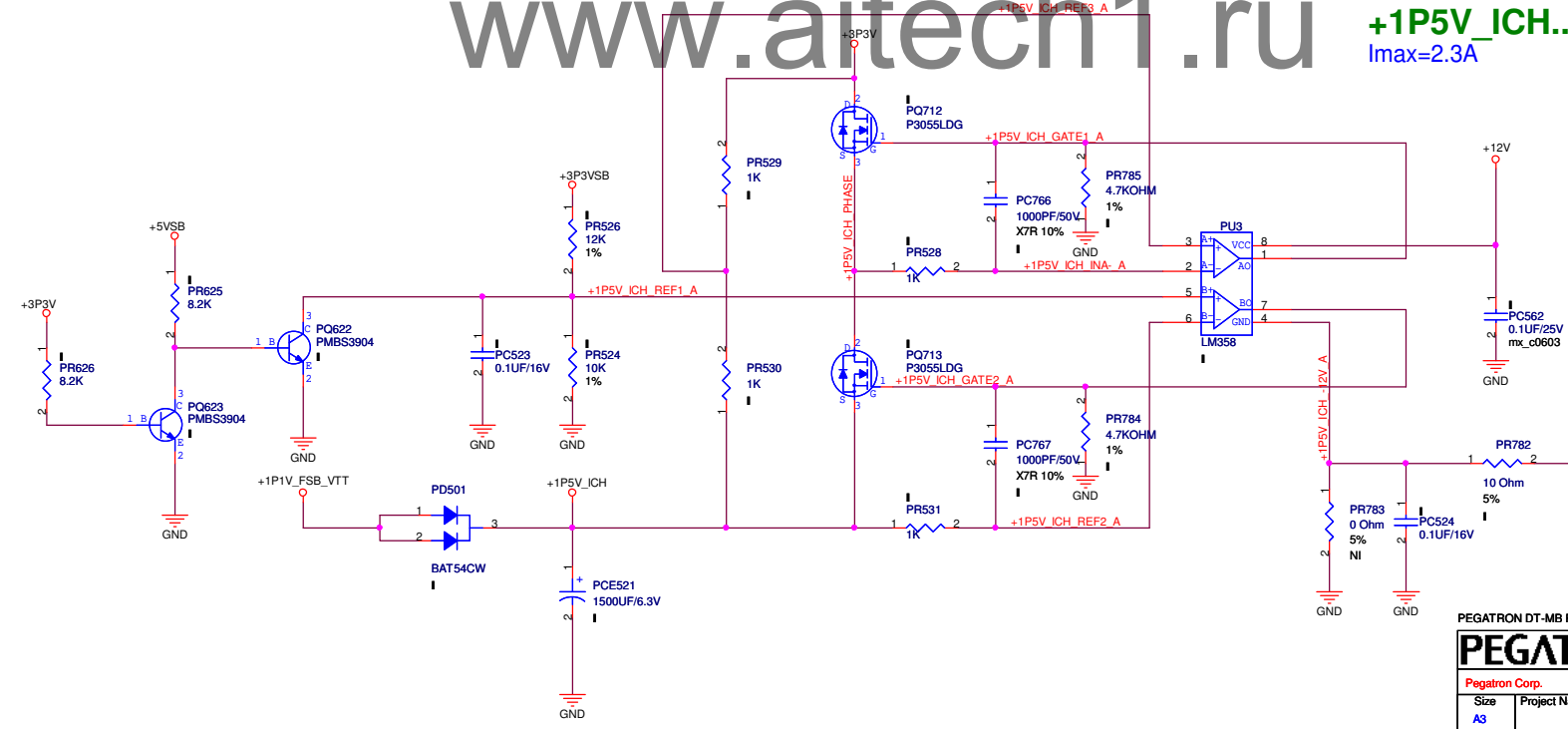
$$V_o = 0.8V(1 + R_{top}/R_{bot})$$

$$2.5V = 0.8V(1 + 47K/22K)$$

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+1P5V_ICH.....(1.5V)

I_{max}=2.3A



PEGATRON DT-MB RESTRICTED SECRET

PEGATRON		Title : +3P3V_CL&1P5V_ICH	
Pegatron Corp.		Engineer: Wesley_Tzeng	
Size	Project Name	ZEUS-80	
A3		Rev 1.05	
Date: Monday, October 12, 2009		Sheet 69 of 74	

[illegible][illegible][illegible]

Schematics Change History -1

Version	Date / Author	Comments
001	2008/01/18	Preliminary release
002	2008/02/13	Change 1394 signal TPA1+ to connector pin 1 & TPA1- to connector pin2 (page.45)
003	2008/02/13	Change CKR37,CKR47 to connect CK_14M_ICH from CK_48M_SIO (page.7)
004	2008/02/13	Remove HR17 (page.9)
005	2008/02/13	Remove HR76,HR77 (page.10)
006	2008/02/13	Add NR10 & NR29 (page.15)
007	2008/02/13	Add PCIEx16 & DVI Switch(M1Q6,M1Q9) (page.24)
008	2008/02/13	Remove SR107 (page.27)
009	2008/02/13	Cut of CPUPWRGD signal on SIO (page.48)
010	2008/02/13	Cut of CPURESER signal on SIO (page.49)
011	2008/02/13	Add SMBus Switch Circuit(page.7.33.58)
012	2008/02/14	Change SR85 to 100k from 10k(page.30)
013	2008/02/14	Cut line between CD1 pin2 & pin3 and AGND(page.36)
014	2008/02/14	Change F3CB2 to connect F3U2 pin8 from from F3U3 pin8(page.47)
015	2008/02/17	RemoveTPM funtion (page.59)
016	2008/02/18	Add PR116, PR129, PR143, PR144, PC119, PC120, PC121, PQ102 for Vcore controller resever (page.63)
017	2008/02/18	Change PCE410, PCE411, PCE412,PCE413, PCE415, PCE416,PR408, PR415 for Eaglelake chip update (page.60)
018	2008/02/18	Add PU500, PC500, PC501, PC506, PC507, PC508, PR500, PR501 for Eaglelake chip update (page.66)
019	2008/02/18	Change PQ300, PCE300,PU300, PC303, PC304 to enable soft-start for +3P3VSB (page.66)
020	2008/02/19	Add O2R23,O2R24 for Samsung(page.49)
021	2008/02/19	Add O2R2(page.49)
022	2008/02/19	Add F1R7 for Samsung(page.55)
023	2008/02/19	Reserve NCB26 (page.14)
024	2008/02/19	Reserve SC15 (page.30)
025	2008/02/19	Change UCE4,UCE6,UCE7,UCE15 to 470uF from 820uF(page.42.43)
026	2008/02/20	Remove SR6 for only instal Intel Lan (page.27)
027	2008/02/20	Add SR6 for not instal USB4(page.28)
028	2008/02/20	Add EC33 for EMI(page.54)
029	2008/02/20	Add ZR26,ZR27 for SMBus Switch (page.58)
030	2008/02/21	Add NCB66 for NB 1P1V_CL (page.16)

PEGATRON DT-MB RESTRICTED SECRET

PEGATRON		Title : CHANGE HISTORY-1	
Pegatron Corp.		Engineer: Wesley_Tzeng	
Size A3	Project Name ZEUS-80	Rev 1.05	
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Schematics Change History –2

Version	Date / Author	Comments
031	2008/02/21	Add PC509,PC510 for decoupling capacitance(page.62)
032	2008/02/21	Add PQ506,PQ507,PR519,PR522 for power sequence(page.62)
033	2008/02/21	Add PC557 decoupling capacitance(page.67)
034	2008/02/21	AddPQ622,PQ623,PQ625,PQ626 for power sequence(page.62)
035	2008/02/21	Add M1R2 for FET stability(page.22)
036	2008/03/17	Change NR54 option to NI,NR55 option to I for nonHDMI(page.15)
037	2008/03/17	Change VR21,VR22 option to NI(page.21)
038	2008/03/17	Add VR23,VCB4(page.21)
039	2008/03/17	Change DVI ESD Protection diode pull-high to 5V(page.25)
040	2008/03/17	Remove SR100 for only Intel LAN(page.31)
041	2008/03/17	Change SR120 option to NI,SR121 option to I for GTL_REF change to 0.63Vtt(page.29)
042	2008/03/17	Remove O2R2(page.49)
043	2008/03/17	Change O2R200 to connect S4_STATE# (page.49)
044	2008/03/17	Move SR45 and change option to NI,change SR46 option to I(page.29)
045	2008/03/17	Change J102,OR70,Q10 option to I(page.55)
046	2008/03/17	Change +1P1V_CORE to connect VccDMI & +1P1V_VR to connect Vcc(page.31)
047	2008/03/17	Add LR2 to Pull-Up LAN_DISABLE_N(page.39)
048	2008/03/18	Remove M1Q2,M1R2 (page.22)
049	2008/03/18	M1Q6 connect to DVI level-shifter Pin9,M1Q9 connect to DVI level-shifter Pin8 (page.22)
050	2008/03/18	Change the PCE700,PCE701 package and change PCE702 option to NI(page.62)
051	2008/03/18	Reserve O2R2,O2R18,O2R22,O2R25,O2R29 to Pull-High & Pull-Down (page.49)
052	2008/03/18	Change PR511 to 4.7K from 0ohm (page.67)
053	2008/03/18	Add PR418,PR426(1.96K)for1.125V (page.60)
054	2008/03/18	Change PR501 to 2.1K from 2.05K (page.66)
055	2008/03/18	Add PR502 for SEC request (page.66)
056	2008/03/18	Change U2 Pin12 NetName to RI1# from DTR1# (page.51)
057	2008/03/19	Change M1R11 to 1K from 8.2K (page.23)
058	2008/03/28	Add EC35 for EMI improvement (page.42)
059	2008/03/28	Add EC36 for EMI improvement (page.43)
060	2008/03/28	Add EC34 for EMI improvement (page.54)

PEGATRON DT-MB RESTRICTED SECRET

PEGATRON		Title : CHANGE HISTORY-2	
Pegatron Corp.		Engineer: Wesley_Tzeng	
Size A3	Project Name ZEUS-80	Rev 1.05	
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Schematics Change History -3

Version	Date / Author	Comments
061	2008/03/28	Add EC37 for EMI improvement (page.54)
062	2008/03/31	Add one decoupling capacitorPC558 (page.66)
063	2008/03/31	Add NR41,NR42,NR43,NC17,NC18,NQ3,NQ4 to improve CLPWROK (page.58)
064	2008/03/31	Change NR91 to 2.7K from 1K for improve CLPWROK (page.58)
065	2008/04/01	Change F1R85 to 10K from 4.7K for follow CRB (page.55)
066	2008/04/01	Change NR4 & NR8 to 49.9ohm from 51ohm for follow CRB (page.11)
067	2008/04/01	Change O2R42 to 8.2K from 4.7K for follow CRB (page.48)
068	2008/04/02	Change SR31 to 8.2K from 4.7K for follow CRB (page.29)
069	2008/04/02	Change SR57,SR77,SR78 to 10K from 8.2K for follow CRB (page.30)
070	2008/04/02	Change OR67,OR68 to 2.2K from 8.2K for follow CRB (page.53)
071	2008/04/02	Change SRN1,SRN2 to 8.2K from 4.7K for follow CRB (page.29)
072	2008/04/07	ChangeVC3,VC6,VC9 to 8.2pF from 3.3pF for improve VGA (page.21)
073	2008/04/16	Add MR31,MR32,MR33,MR34 pull-high to improve DVI (page.24)
074	2008/04/16	Change MR30 to 499ohm from 1.2K for improve DVI (page.24)
075	2008/04/24	Add O2R31 pull-down for SEC request (page.49)
076	2008/04/24	Move AR25 to solve Audio noise issue (page.55)
077	2008/04/28	Add LR35,LR36,LD1 to reserve LAN LED control (page.39,40)
078	2008/05/05	Change PR416,PR422 to 1.33K from 806 OHM to meet the Intel G45 1.125V±30mV specification (page.60)
079	2008/05/05	Change PR417 to 100 ohm from 14 ohm to meet the Intel G45 1.125V±30mV specification (page.60)
080	2008/05/05	Change PR419 to 12K from 2.74K to meet the Intel G45 1.125V±30mV specification (page.60)
081	2008/05/05	Change PR415,PR408 to 3.24K from 2.1K to meet the Intel G45 1.125V±30mV specification (page.60)
082	2008/05/05	Change PR418,PR426 to 3.48K from 1.96K to meet the Intel G45 1.125V±30mV specification (page.60)
083	2008/05/05	Change PC407 to 47nF from 0.068uF to meet the Intel G45 1.125V±30mV specification (page.60)
084	2008/05/05	Change PC408 to 2200pF from 0.033uF to meet the Intel G45 1.125V±30mV specification (page.60)
085	2008/05/05	Change PC409 to 47pF from 2200pF to meet the Intel G45 1.125V±30mV specification (page.60)
086	2008/05/06	Change ICH10 Pin AK27 pull-downm to follow CRB (page.32)
087	2008/05/08	Change PR520 to 100K ohm from 68.1K to solve +1P1V_FSB_VTT margin issue (page.61)
088	2008/05/27	Change HR70,HR72 to 10K ohm from 1K to improve component stress (page.8)
089	2008/05/27	Change NR60 to 88.7ohm from 40.2ohm,NR62 to 86.6 ohm from39.2 ohm to improve component stress (page.16)
090	2008/05/27	Change SR93 to 22 ohm from 10 ohm,SCB5 to 1uF from 0.1uF to solve USB ESD issue (page.31)

PEGATRON DT-MB RESTRICTED SECRET

PEGATRON		Title : CHANGE HISTORY-3	
Pegatron Corp.		Engineer: Wesley_Tzeng	
Size A3	Project Name ZEUS-80	Rev 1.05	
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